

Colossus 15/17 DIS_OPT Schematic IVY Bridge (rPGA989) Intel PCH (Panther Point)

REV:-1
2012-01-05.

DY:No stuff
DIS_OPT:DISCRTE OPTIMUS installed
DY_35W:No stuff on 35W CPU
DY_45W:No stuff on 45W CPU
CR_Balen17:Stuff for 17"
CR_Goya:Stuff for 15"

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

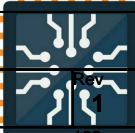
Size
A4

Document Number

Colossus

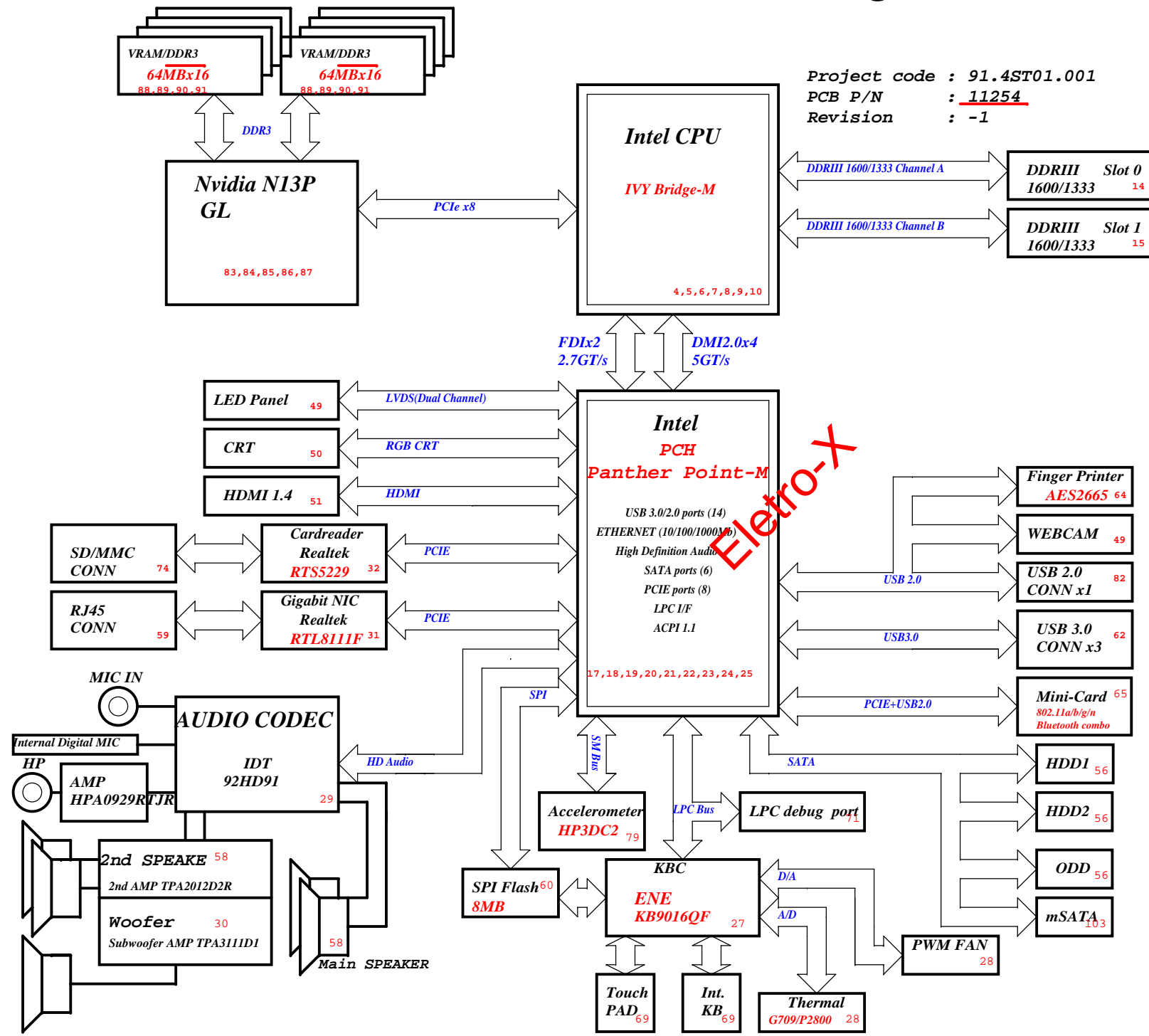
Date: Wednesday, January 04, 2012

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ECE-RO-2

COLOSSUS Block Diagram



SYSTEM DC/DC TPS51461 48		CPU DC/DC VT1323 42~44	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
5V_S5	VCCSA=0D85V_S0	DCBATOUT (5V_S5)	VCC_CORE

SYSTEM DC/DC SN1003055RUWR 45	
INPUTS	OUTPUTS
5V_S5/3D3V_S5	1D05V_S0

SYSTEM DC/DC RT8223M_5V/3D3V 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207MZ 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

GFX DC/DC VT1323 42~44	
INPUTS	OUTPUTS
DCBATOUT (5V_S5)	VCC_GFXCORE

VGA NCP3218G 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24738 40	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

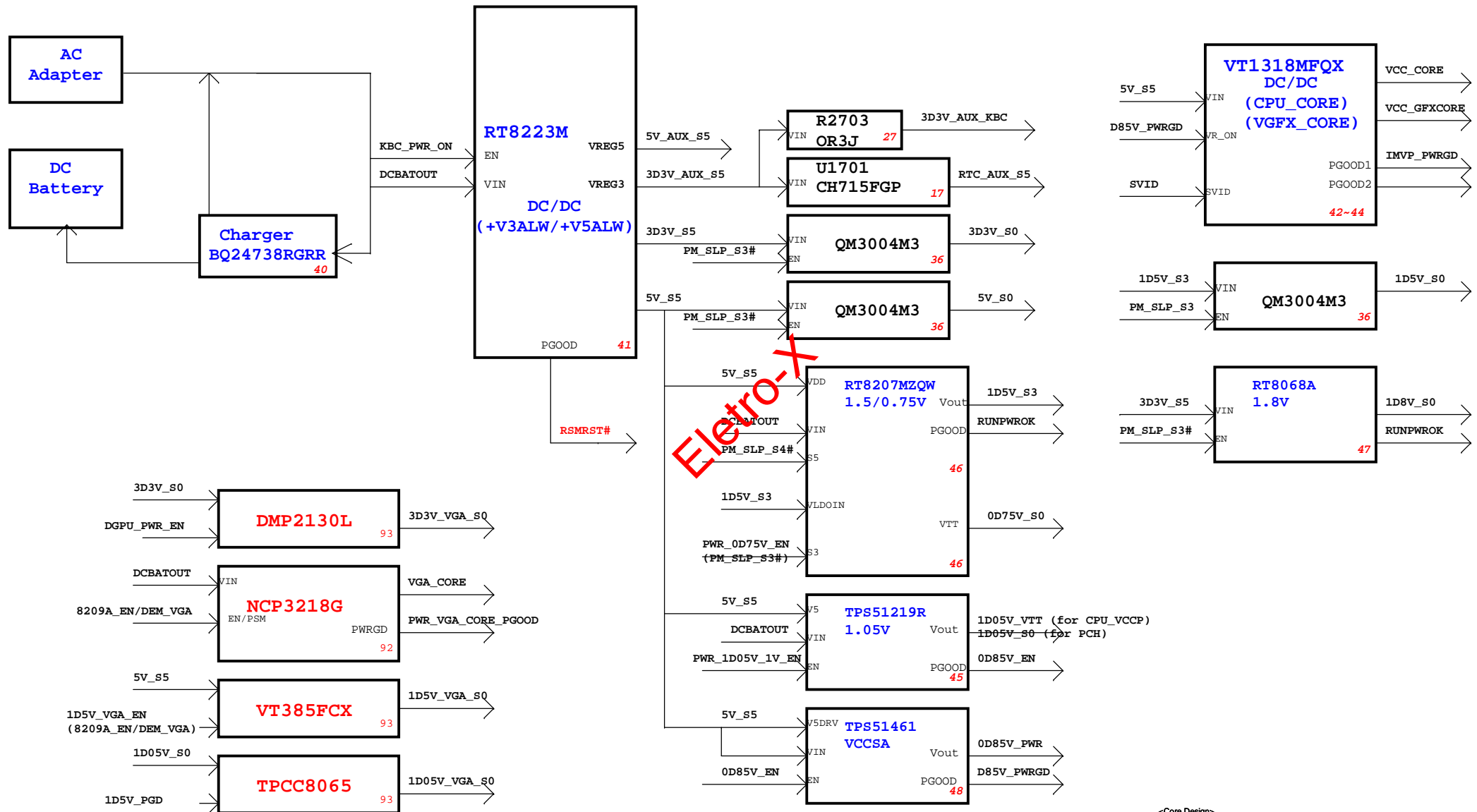
SYSTEM DC/DC RT8068A 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC VT385FCX 93	
INPUTS	OUTPUTS
3D3V_S0 1D5V_S0 1D5V_S3	3D3V_VGA_S0 1D5V_VGA_S0 1V05_VGA_S0

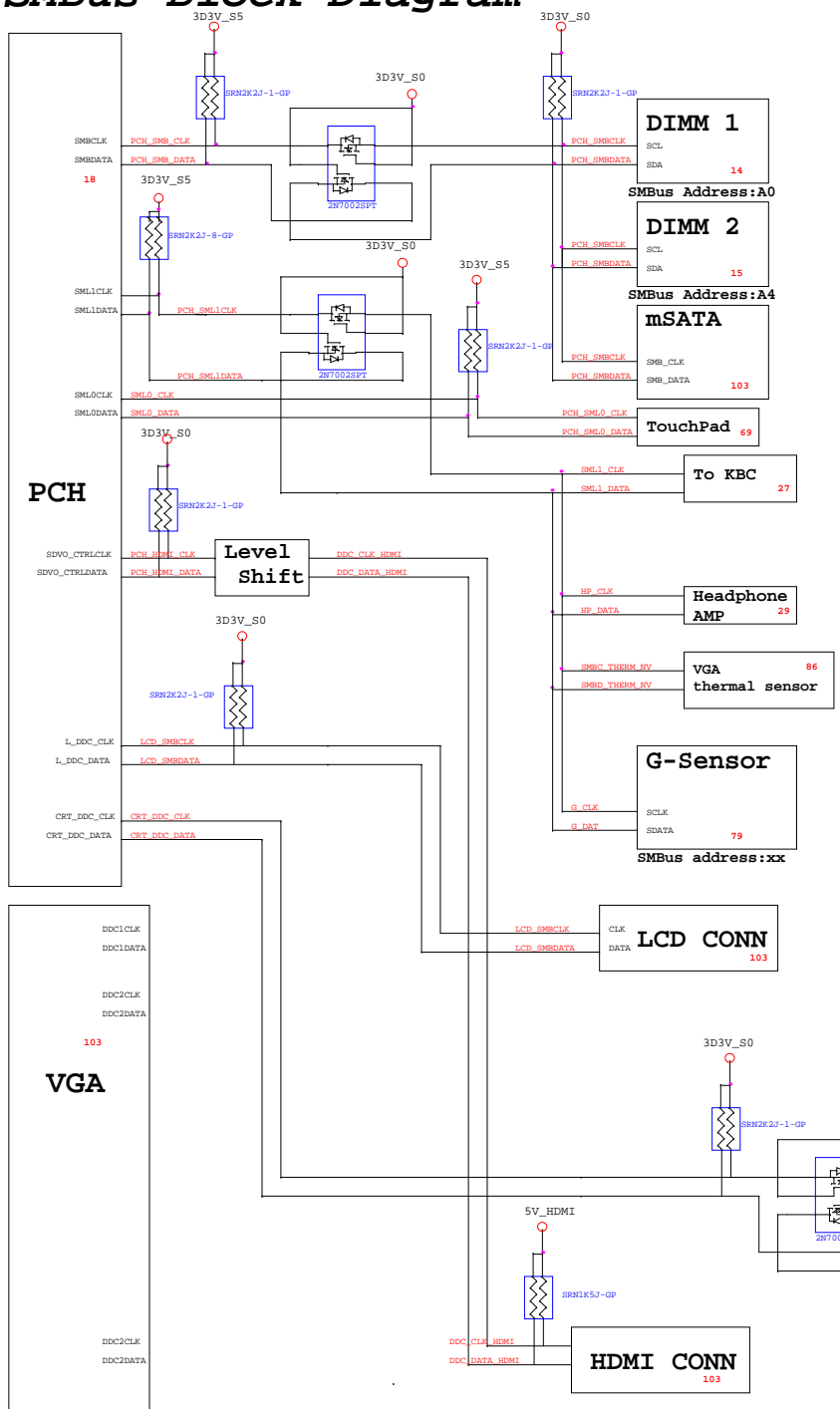
Switches 36	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB LAYER (DISCRETE)	
L1:Top L2:GND L3:Signal L4:Signal	L5:VCC L6:Signal L7:GND L8::Bottom

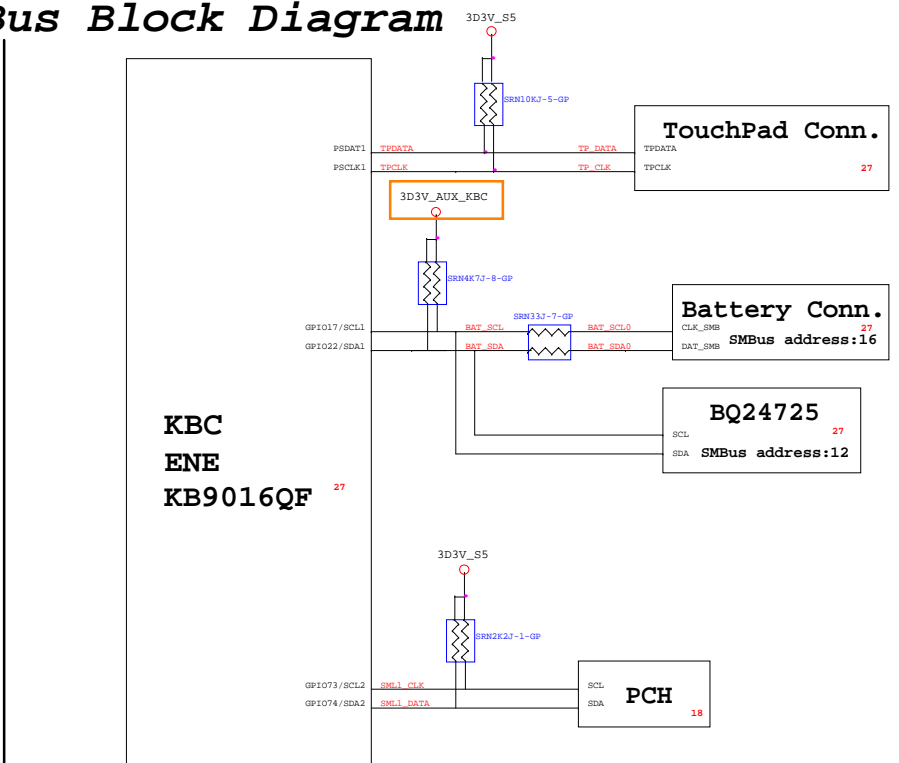
COLOSUSS POWER BLOCK DIAGRAM



PCH SMBus Block Diagram

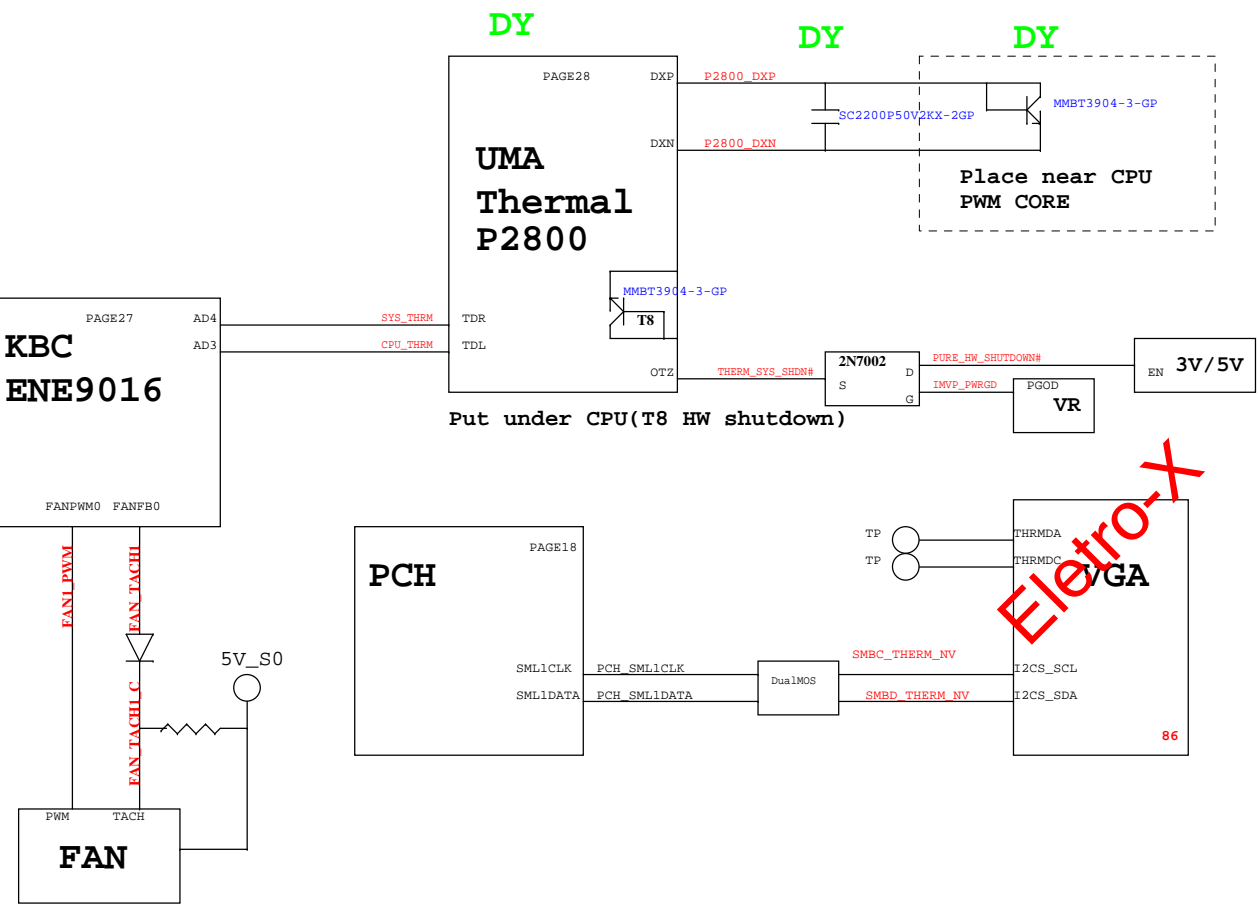


KBC SMBus Block Diagram

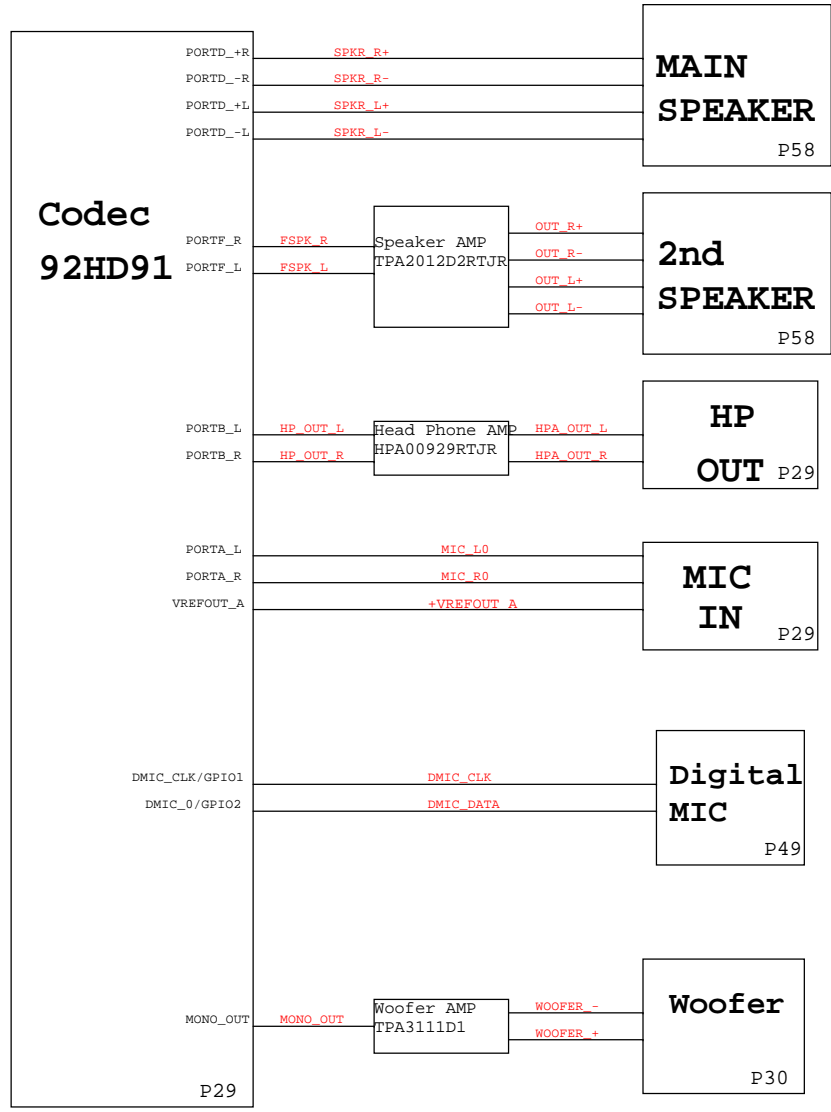


Eleetro-X

Thermal Block Diagram



Audio Block Diagram



PCH Strapping Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIe Routing

LANE1	N/A
LANE2	17"Card Reader
LANE3	15"Card Reader
LANE4	Mini Card1(WLAN)
LANE5	N/A
LANE6	Intel GBE LAN / LAN
LANE7	N/A
LANE8	N/A

USB2.0 Table

Pair	Device
0	USB 3.0 I/O CONN. 1
1	N/A
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN.
10	Camera
11	FREE
12	FREE
13	FREE

USB3.0 Table

USB	
Pair	Device
1	I/O CONN. 1
2	FREE
3	I/O CONN. 2
4	I/O CONN. 3

Processor Strapping Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to Embedded DisplayPort. 1: Embedded DisplayPort. 0: Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_S0 VCCSA_OD85V OD75V_S0 VCC_CORE VCC_SFPCORE 3D3V_VGA_S0 1D5V_VGA_S0 1D05V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 ~ 1.25V 3.3V 1.5V 1D05V	S0	CPU Core Rail Graphics Core Rail
5V_USBX 1D5V_S3 DDR_VDD_S3	5V 1.5V 0.75V	S3	
5V+ D0P+TOUT _S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3	ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN	ON for iAMTLegacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

SMBus ADDRESSES

I 2 C / SMBus Addresses		Ref Des	Chief River CRV	
Device			Address	Hex Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SMML_CLK/SMML_DATA SMML_CLK/SMML_DATA SMML_CLK/SMML_DATA
PCH SMBus SO-DIMM (SPD) SO-DIMM (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	HDD2
3	N/A
4	ODD
5	N/A

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Title			
Table of Content			
Size	Document Number		Rev
A3	Colossus		1
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CPU(1/7)

IVY BRIDGE PROCESSOR (DMI,DP,PEG,FDI)

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

DP Compensation, within 500mil

NOTE: EDP_HPD
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns.
If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-up resistor on the motherboard.
This signal can be left as no connect if entire eDP interface is disabled.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE:
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

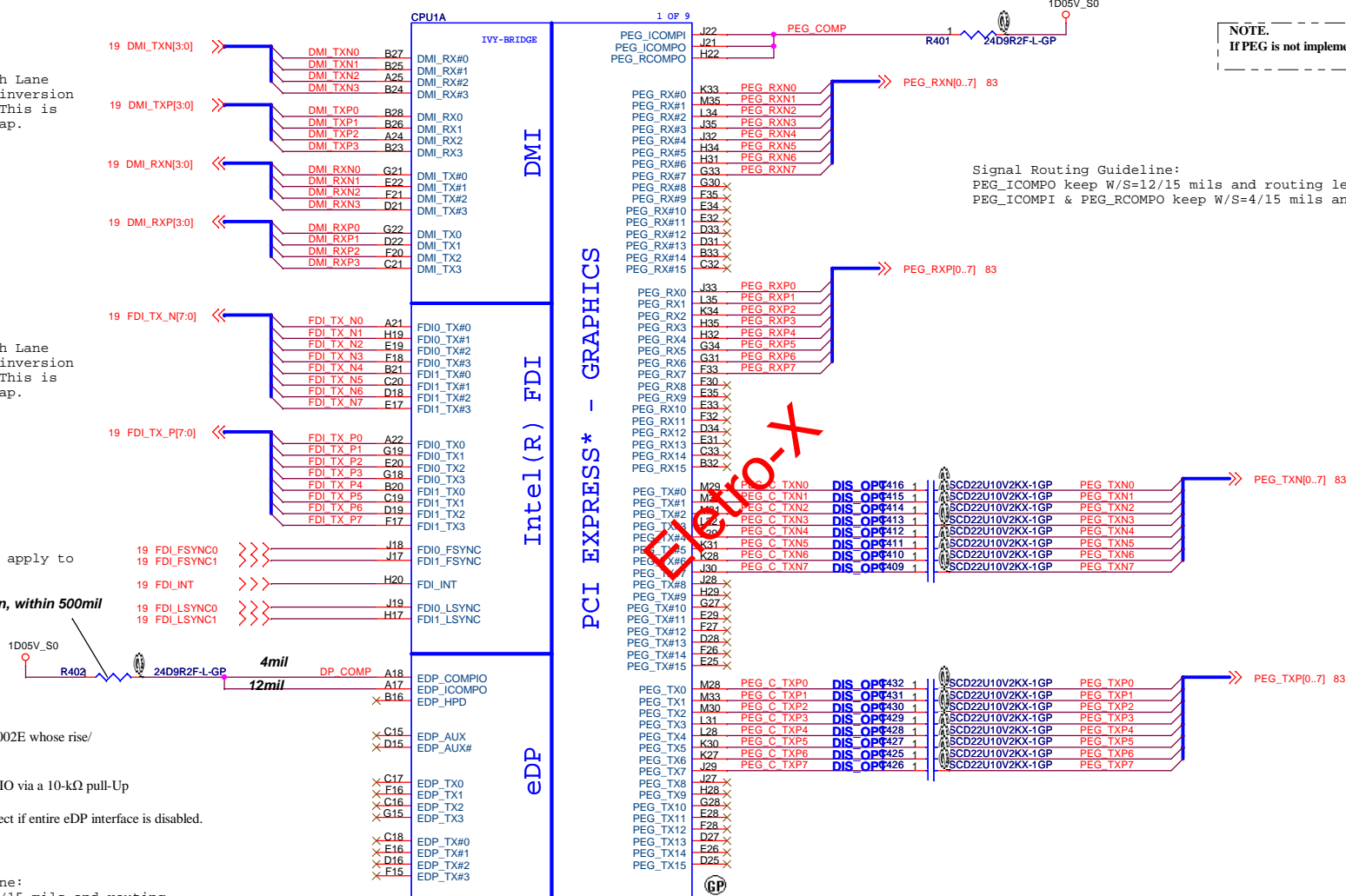
2ND = 62.10055.321
3RD = 62.10055.551

1st 633996-302
2nd 633996-501
3rd 633996-301

PEG Compensation

NOTE:
If PEG is not implemented, the RX&TX pairs can be left as No Connect

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



633996-302

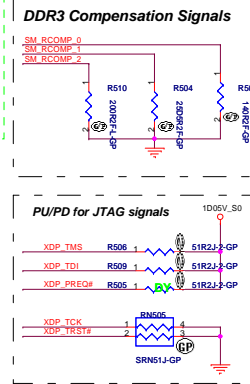
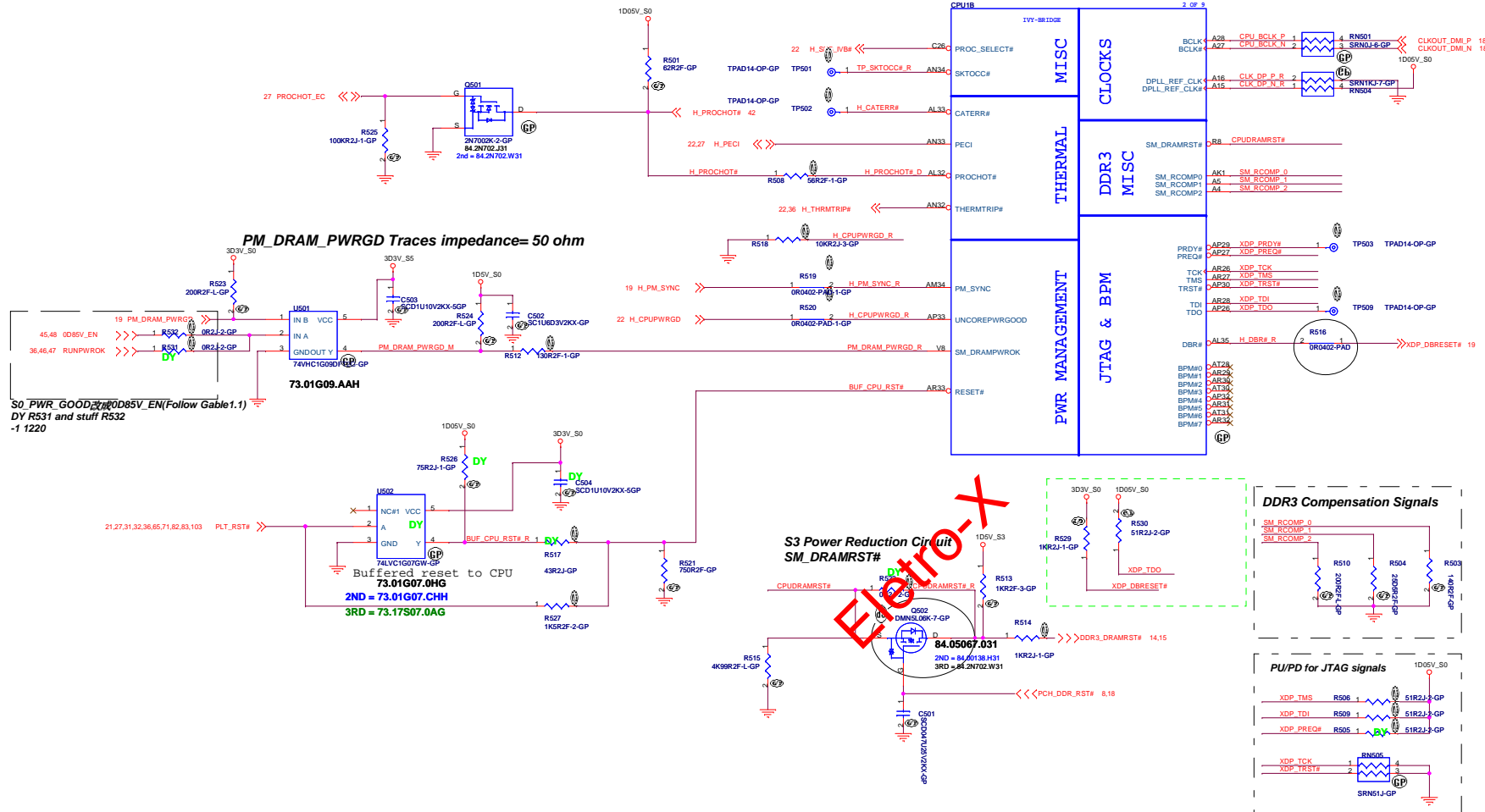
Hand control CPU1 P/N

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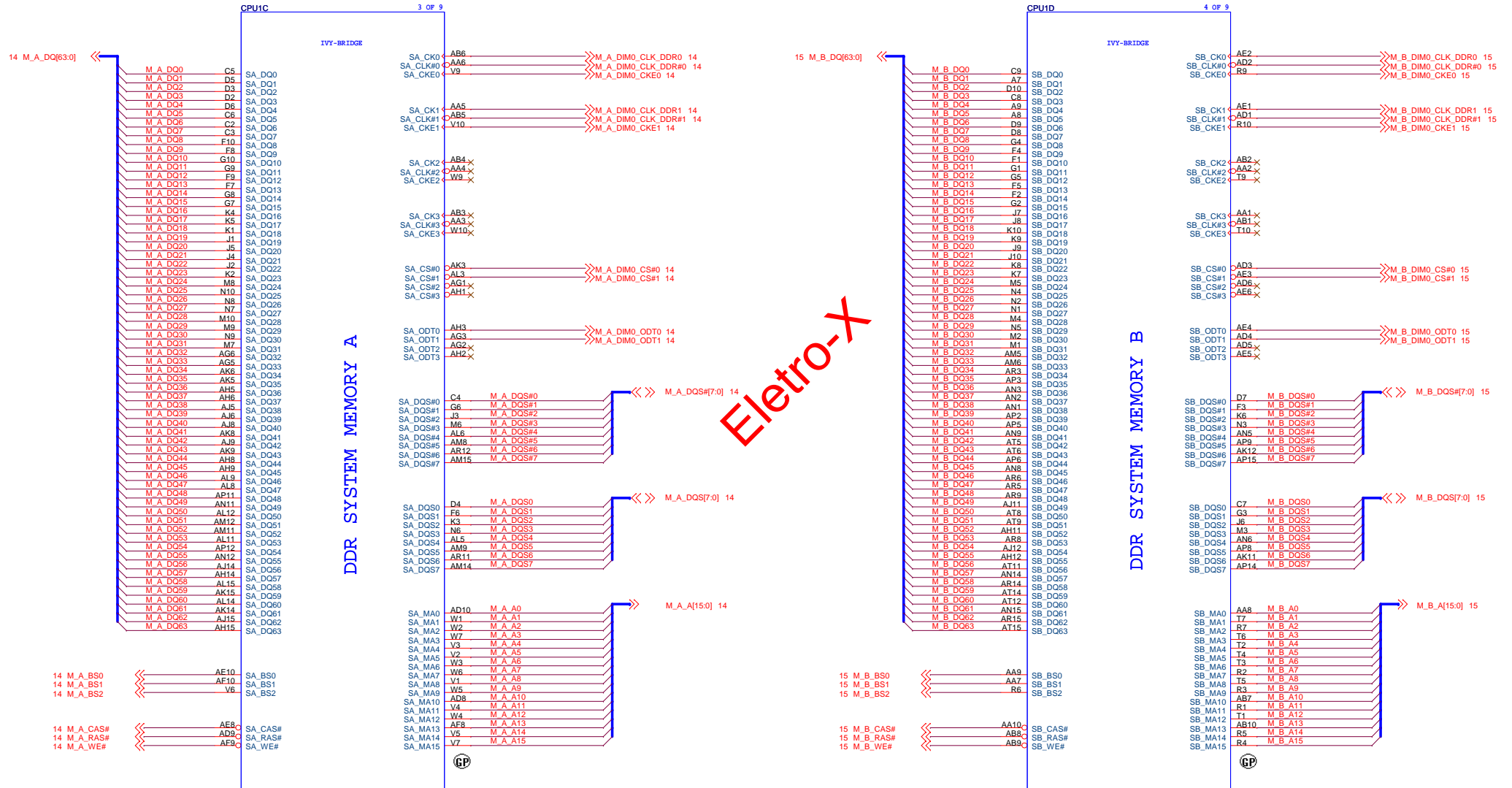
CPU(1/7): DMI/PEG/FDI			
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IVY BRIDGE PROCESSOR (CLK,MISC,JTAG)



CPU(3/7)

IVY BRIDGE PROCESSOR (DDR3)



<Core Design>

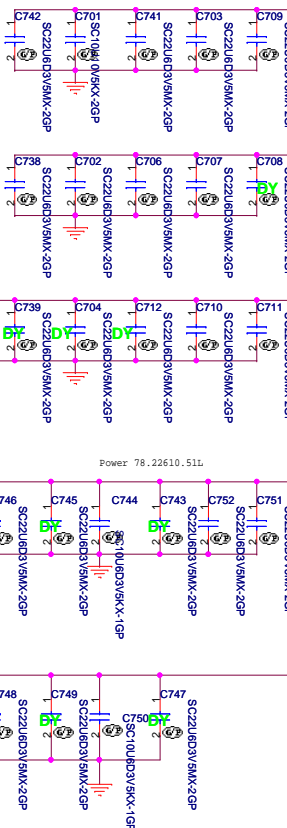
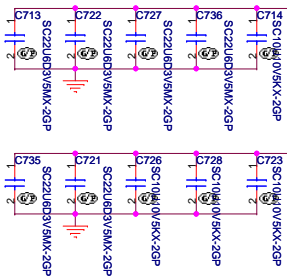
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Custom	Colossus	1	
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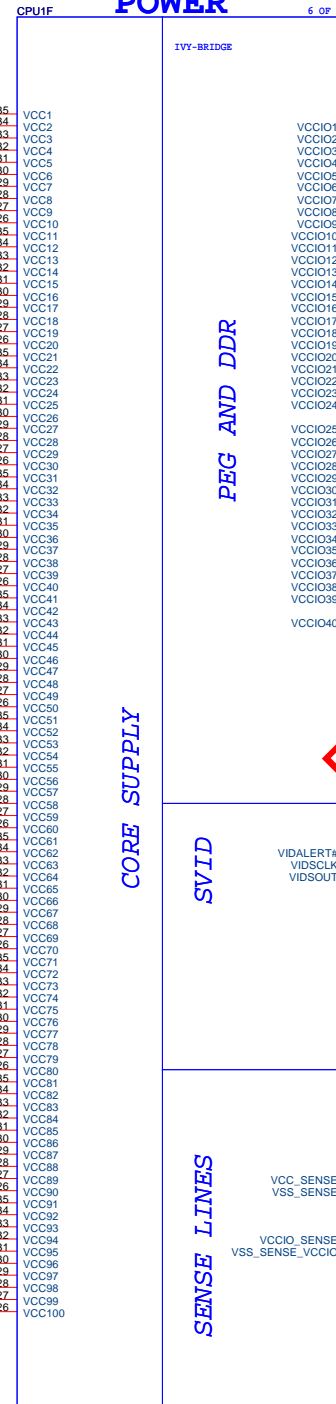
CPU(4/7)

IVY BRIDGE PROCESSOR (POWER)

PROCESSOR CORE POWER



POWER



IVY-BRIDGE

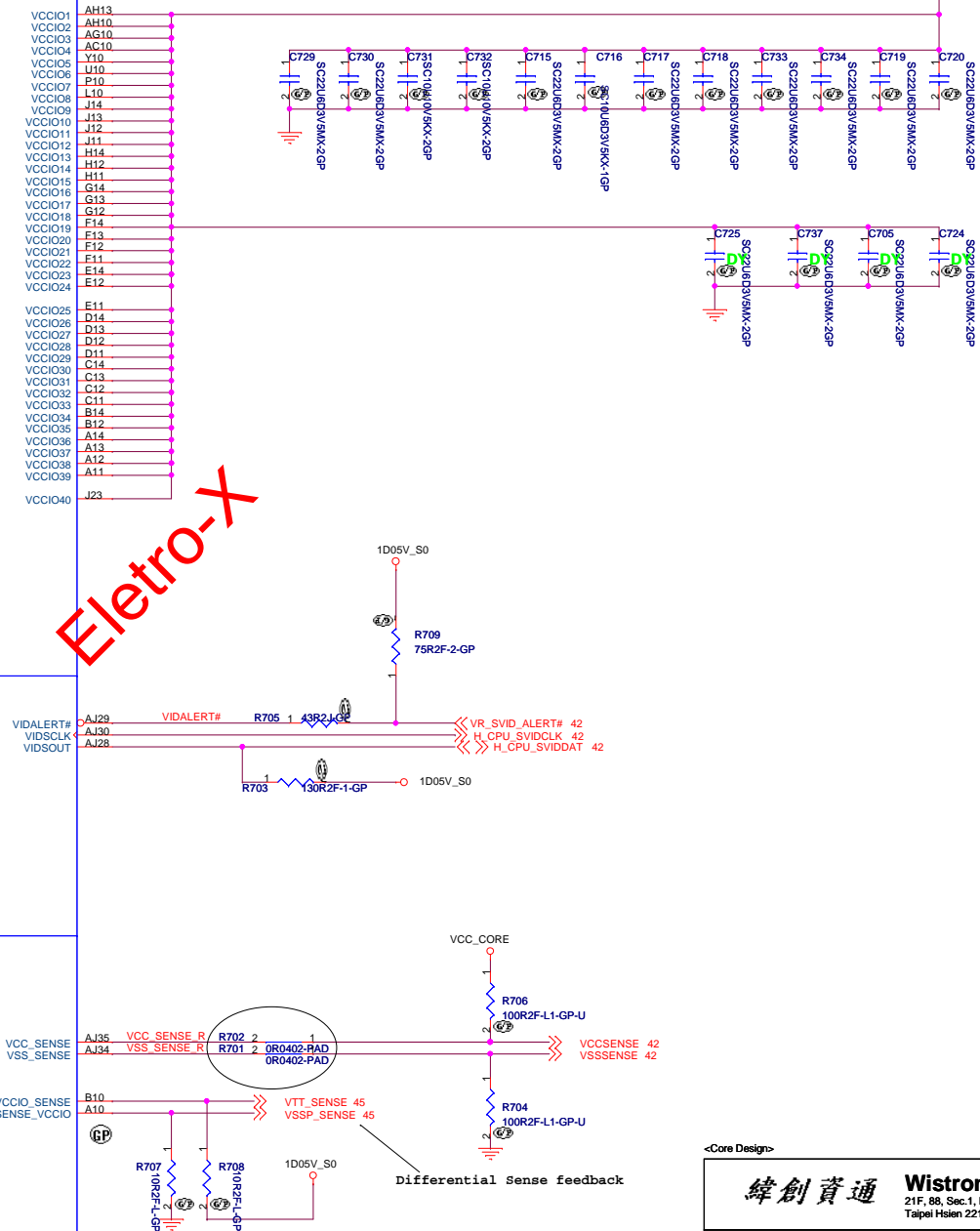
PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

PROCESSOR UNCORE POWER



<Core Design>

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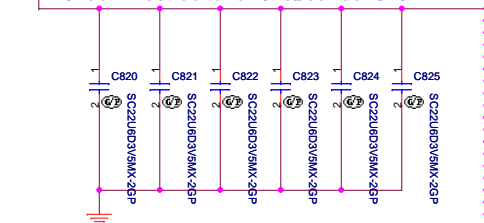
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Size	Document Number			Rev
Custom		Colossus		1
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CPU(5/7) IVY BRIDGE PROCESSOR (GRAPHICS POWER)

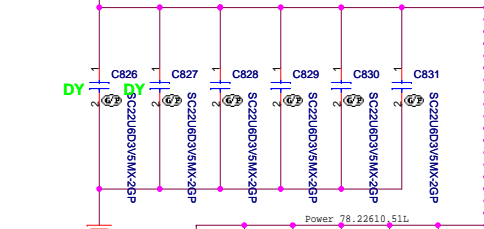
M3 - Processor Generated SO-DIMM VREF_DQ

33A

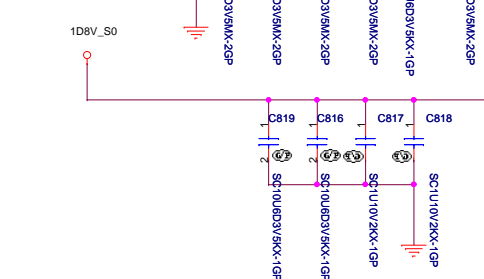
VCC_GFXCORE 470U*2 22U*6
Under Socket and Closed to CPU



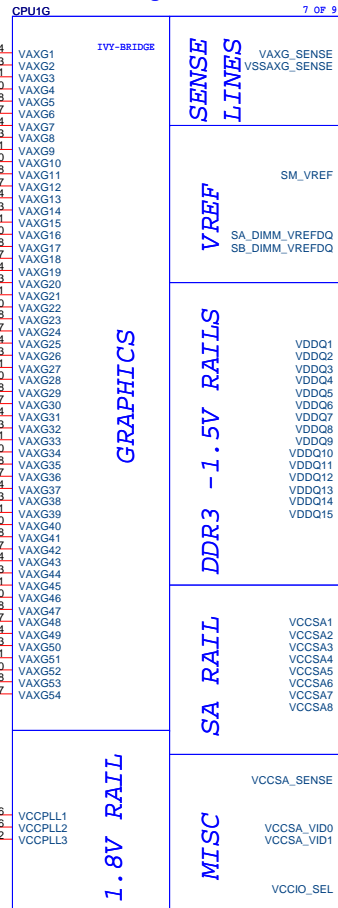
VCC_GFXCORE 22U*6
Closed to CPU Socket



1.5A



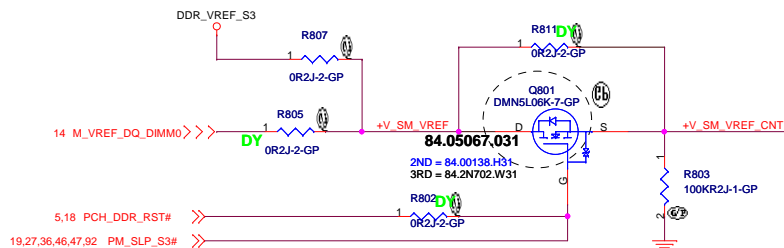
POWER



H_VCCP_SEL	Voltage
1	1.05V
0	1.0V

Eletron-X

S3 Power Reduction Circuit Processor VREF_DQ Implementation



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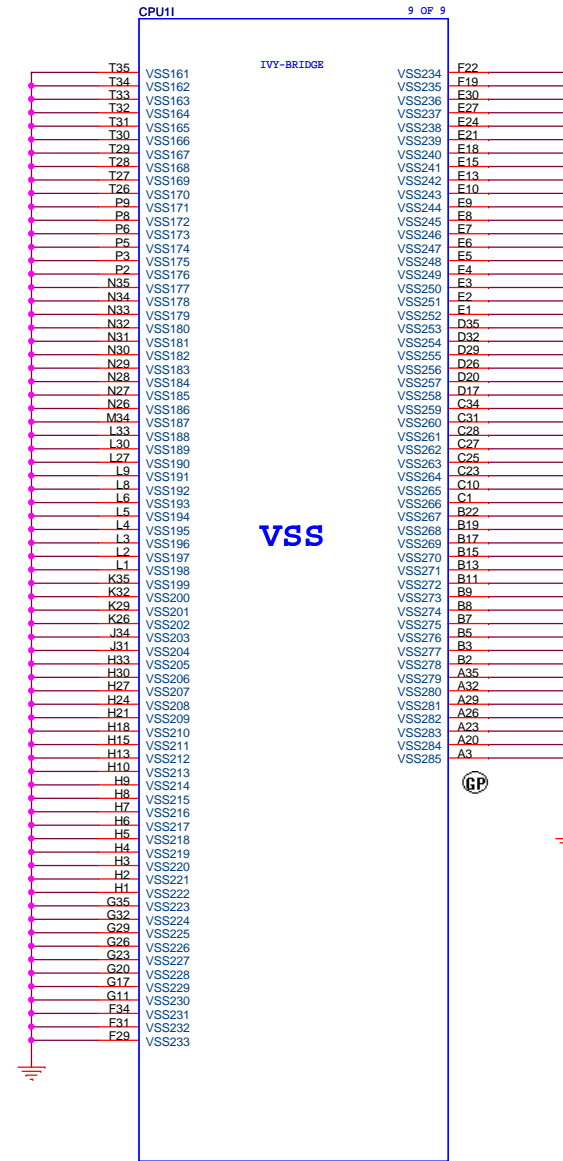
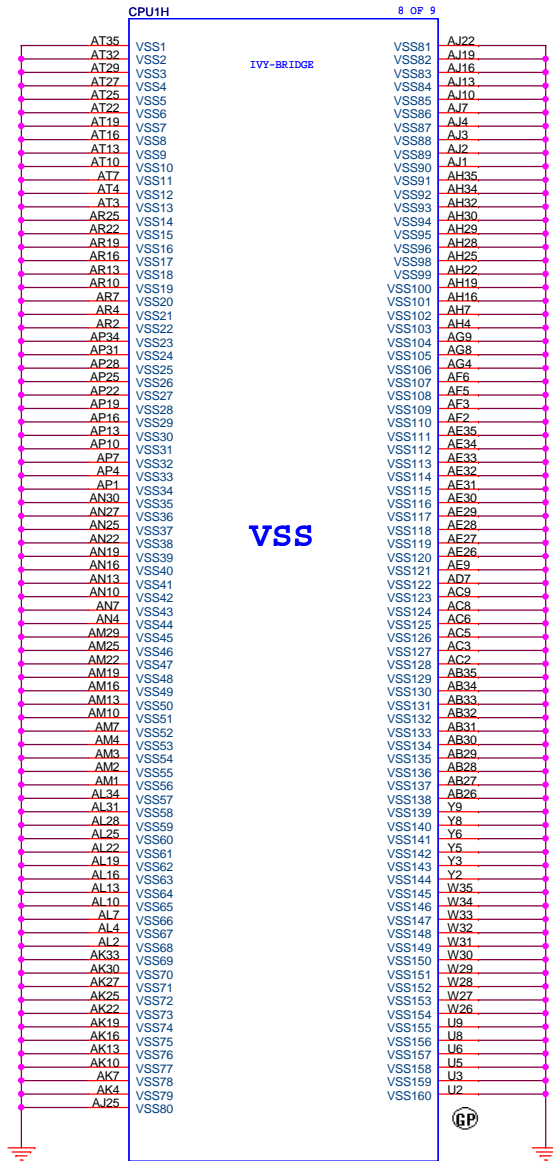
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Size: Custom Document Number: **Colossus** Rev: **1**

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CPU(6/7)

IVY BRIDGE PROCESSOR (GND)



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Title

CPU (6/7):GND

Size
A3

Document Number

Colossus

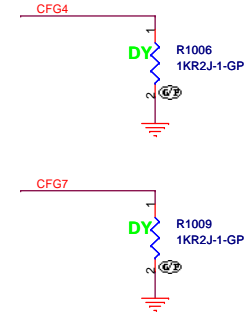
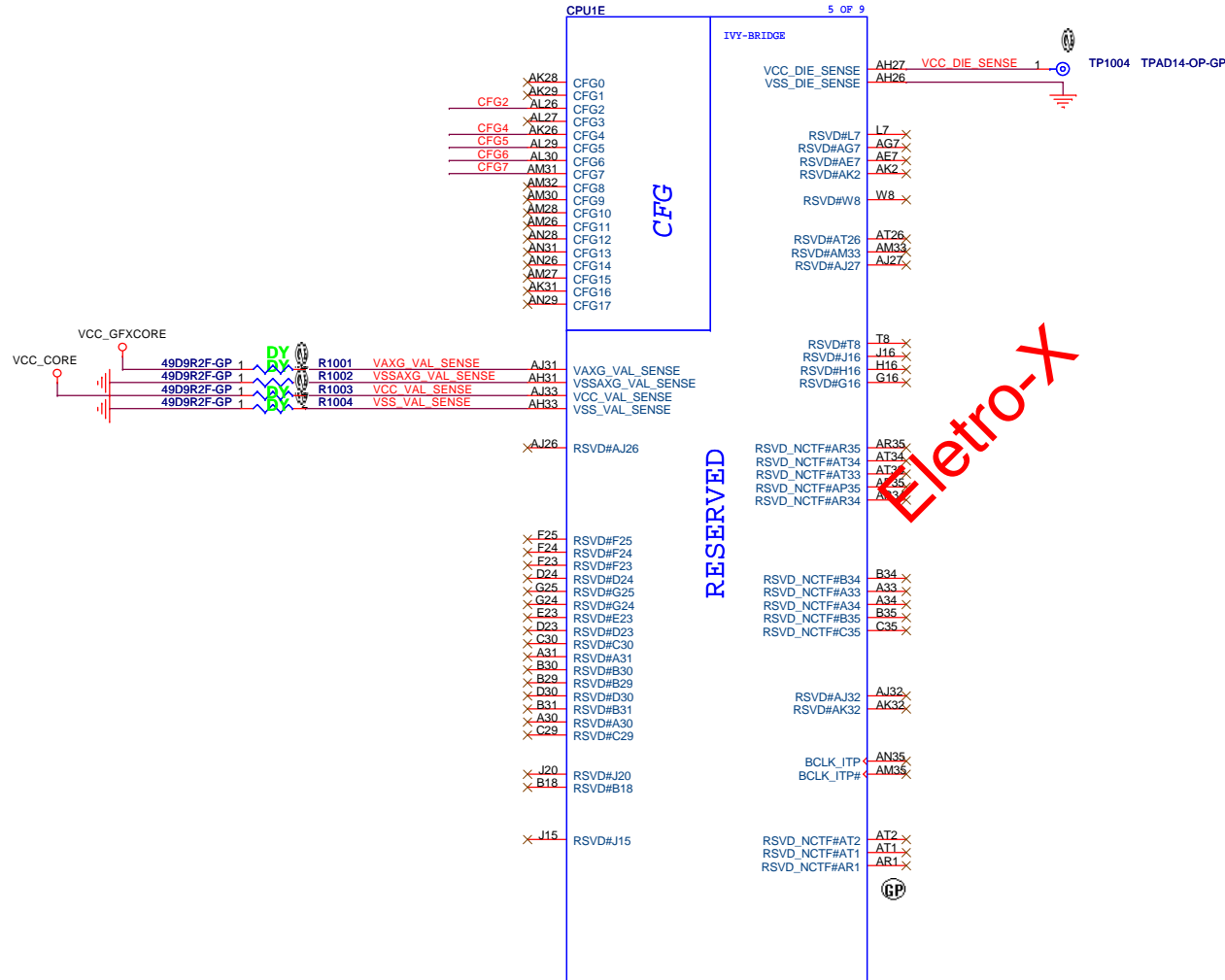
Rev
1

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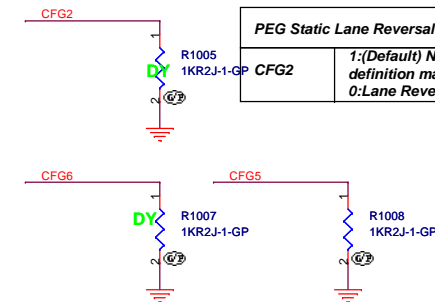
CPU(7/7)

IVY BRIDGE PROCESSOR (RESERVED)



Display Port Presence Strap	
CFG4	1: (Default) Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



PEG Static Lane Reversal	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

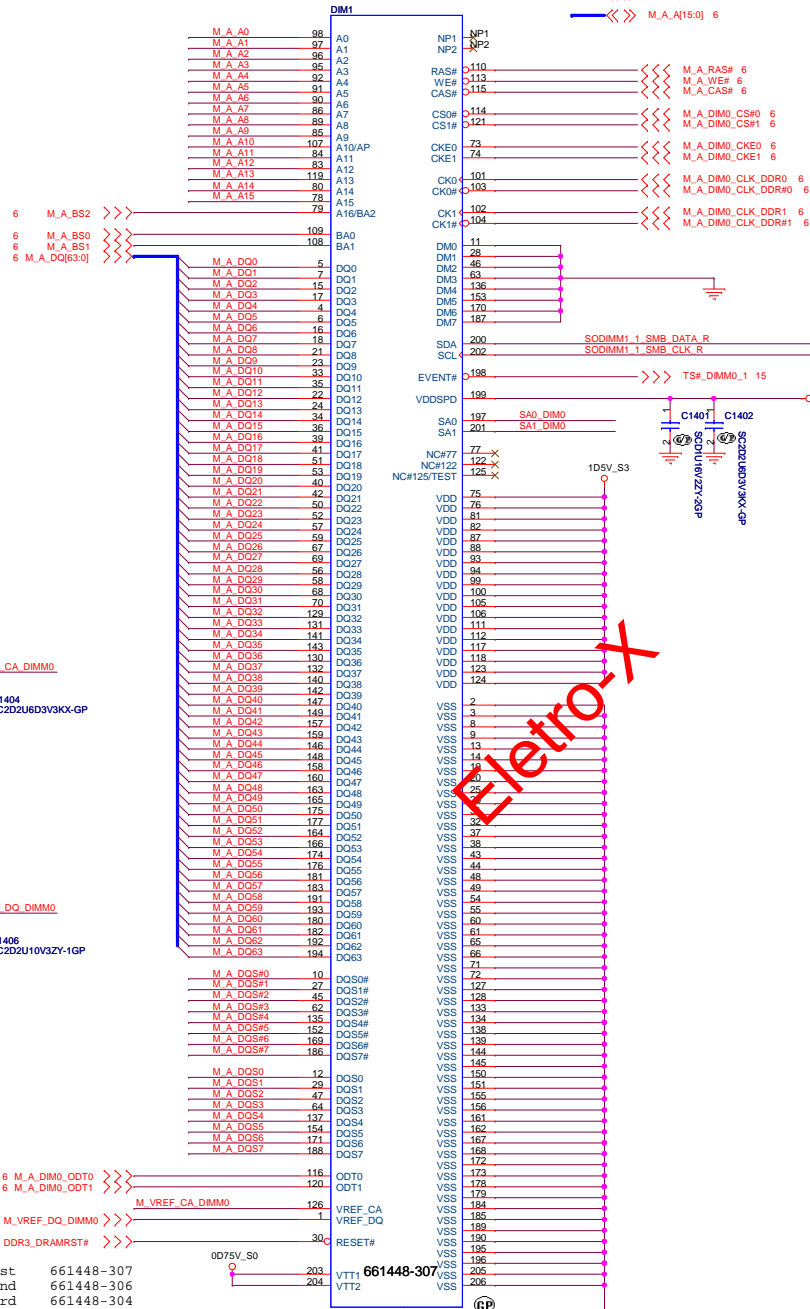
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Title		
CPU(7/7): CFG/RSVD/DDR3 VRE		
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DIMM1 REVERSED

M_A_DQS#7[0] 6
 M_A_DQS#7[0] 6
 M_A_A[15:0] 6



Note:
 If SA0_DIM0 = 0, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA0
 SO-DIMMA TS Address is 0x30
 If SA0_DIM0 = 1, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA2
 SO-DIMMA TS Address is 0x32

Thermal EVENT

SODIMM A DECOUPLING

Layout Note:
 Place these Caps near
 SO-DIMMA.

Place these caps
 close to VTT1 and
 VTT2.

010412 Update connector HP P/N,
 handle control but not change library

H=9.2mm

62.10017.U01
 2nd = 62.10017.U01
 3rd = 62.10024.H81

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Title			Rev
DDR3 SO-DIMM1			1
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DIMM2 REVERSED

6 M_B_A[15:0] <<<>>>
6 M_B_DQS[7:0] <<<>>>
6 M_B_DQS[7:0] <<<>>>

6 M_B_BS2 <<<>>>
6 M_B_BS0
6 M_B_BS1
6 M_B_DQ[63:0] <<<>>>

M_B_A0 96
M_B_A1 97
M_B_A2 98
M_B_A3 99
M_B_A4 100
M_B_A5 101
M_B_A6 102
M_B_A7 103
M_B_A8 104
M_B_A9 105
M_B_A10 106
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M_B_BS1 114
M_B_DQ[63:0] 115

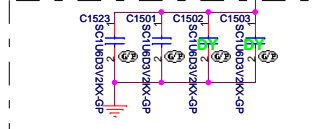
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M_B_DQS#4 81
M_B_DQS#5 99
M_B_DQS#6 117
M_B_DQS#7 135

M_B_DQS0 12
M_B_DQS1 29
M_B_DQS2 47
M_B_DQS3 65
M_B_DQS4 83
M_B_DQS5 101
M_B_DQS6 119
M_B_DQS7 137

6 M_B_DIM0_ODT0 <<<>>>
6 M_B_DIM0_ODT1 <<<>>>
M_VREF_CA_DIMM1 126
8 M_VREF_DQ_DIMM1 <<<>>>
5,14 DDR3_DRAMRST# <<<>>>

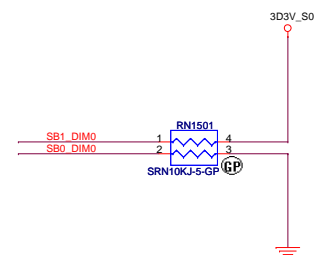
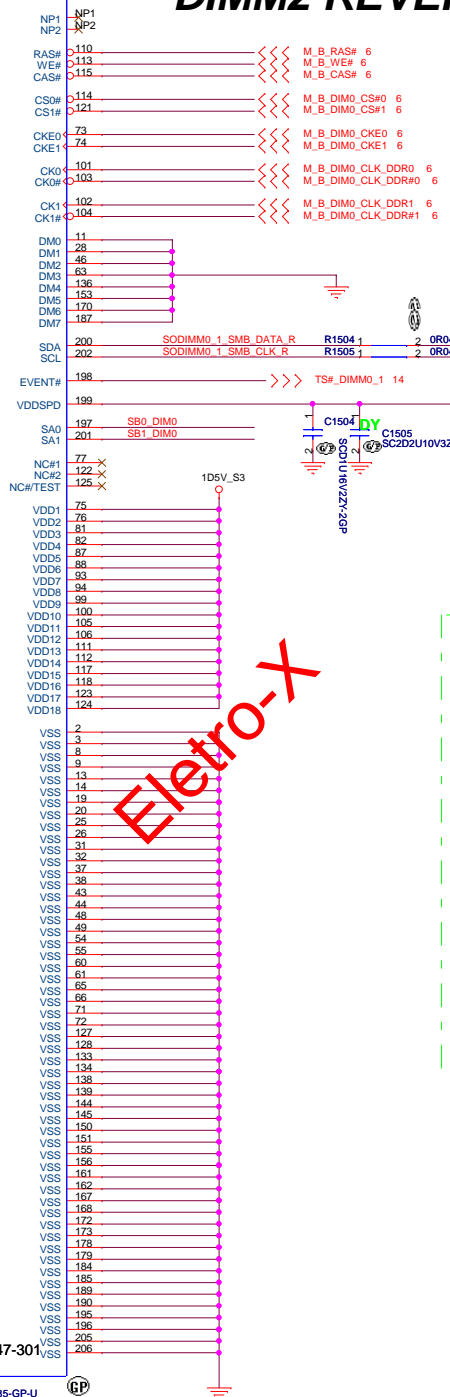
Place these caps close to VTT1 and VTT2.



1st 661447-301
2nd 661447-306
3rd 661447-304

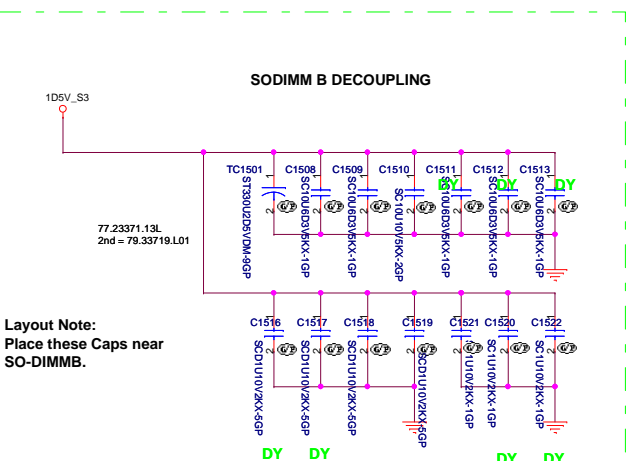
010412 Update connector HP P/N,
hanle control but not change library

62.10017.U21
2ND = 62.10017.T91
3rd = 62.10024.I61
H=5.2mm



Note:
SO-DIMM SPD Address is 0xA4
SO-DIMM TS Address is 0x34

Eleetro-X

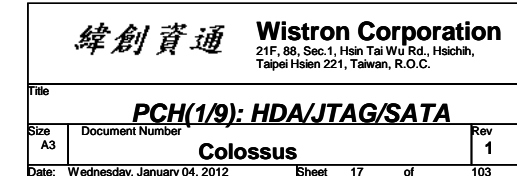


Layout Note:
Place these Caps near SO-DIMM.

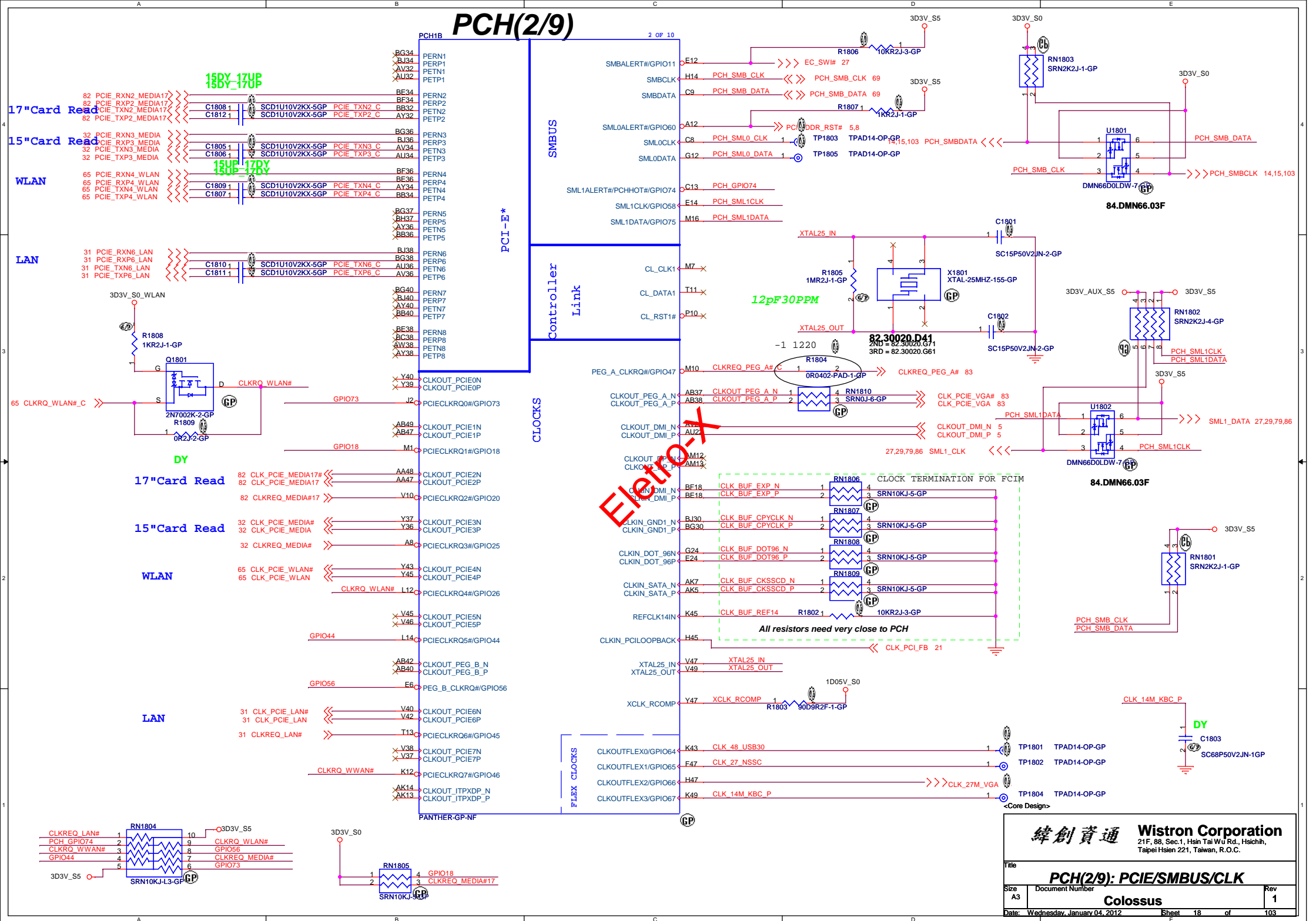
<Core Design>

緯創資通 Wistron Corporation 2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
DDR3 SO-DIMM2	
Size	Document Number
Custom	Colossus
Date: Wednesday, January 04, 2012	Sheet 15 of 103

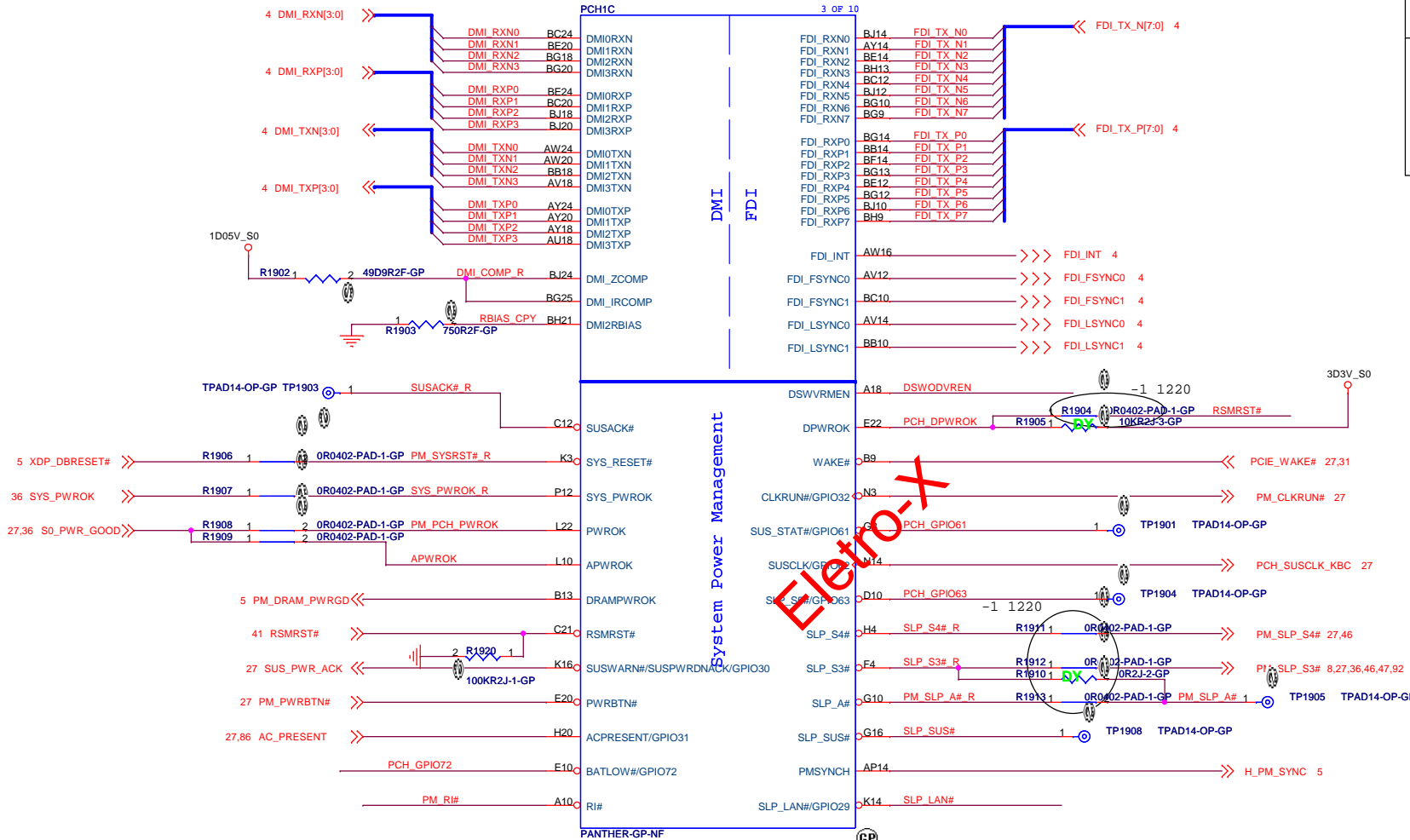
INTVRMEN- Integrated
SUS 1.05V VRM Enable
High - Enable internal VRs



PCH1B 2 OF 10



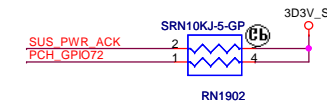
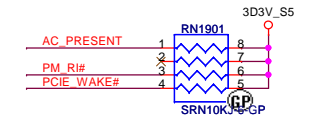
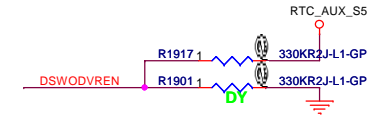
PCH(3/9)



Intel ME-EC Interaction Signal List with and without M3 support

Signal Name	Platform With M3 Support (e.g., Intel AMT)	Platform Without M3 Support
SUSPWRDNACK(GPIO30)	Required	Required
ACPRESENT(GPIO31)	Required	Required
SLP_A#	Required	(Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_A# becomes required from Intel ME-EC prespecrive.

DSWODVREN - On Die DSW VR Enable	
HIGH (R1917 STUFFED, R1901 UNSTUFFED)	Enabled (DEFAULT)
LOW (R1917 UNSTUFFED, R1901 STUFFED)	Disabled

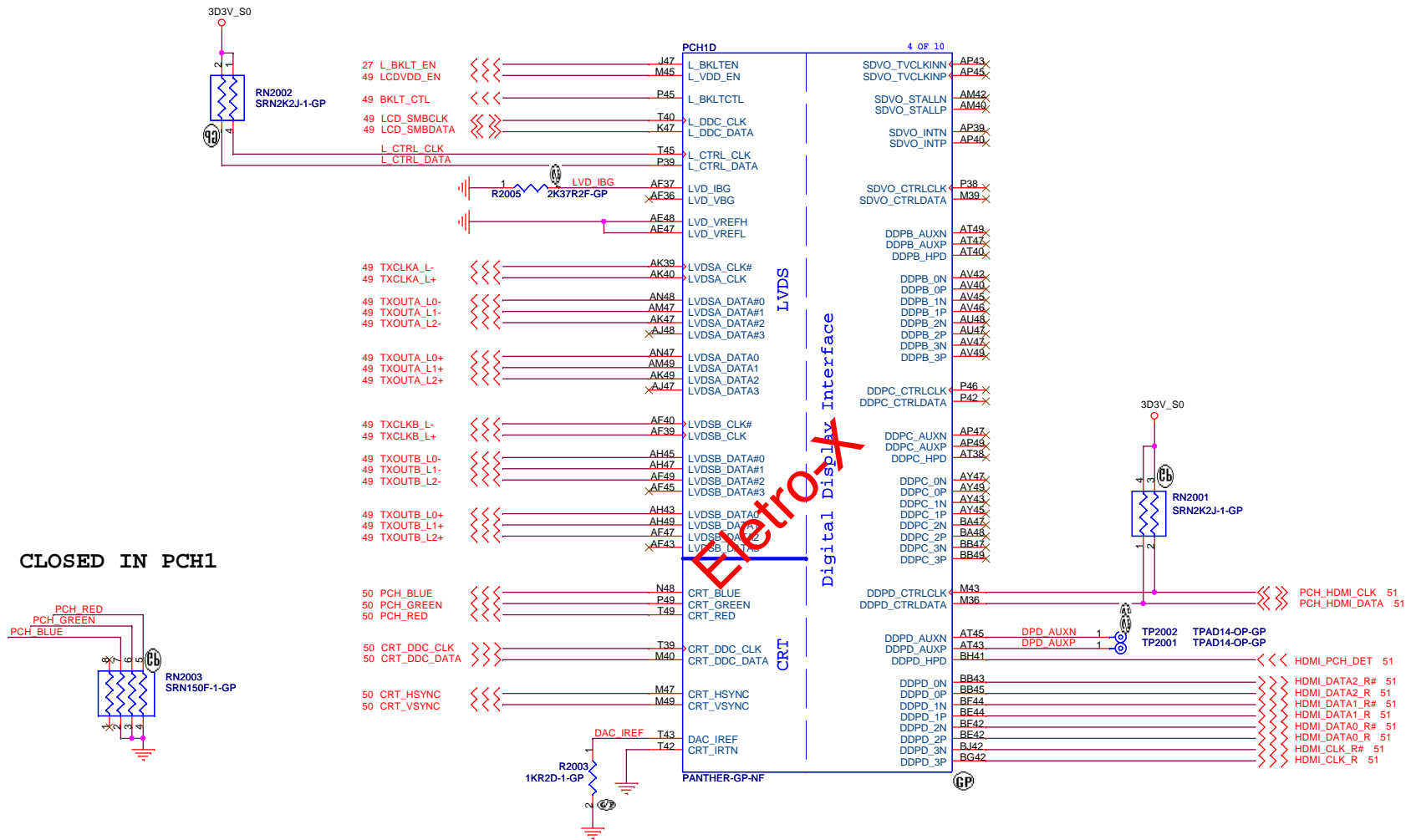


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Title PCH(3/9): DMI/FDI/PM		
Size A3	Document Number Colossus	Rev 1
Date: Wednesday, January 04, 2012 Sheet 19 of 103		

PCH(4/9)



<Core Design>

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Title

PCH(4/9): LVDS/CRT/DDI

Size

Document Number

Colossus

Rev

1

Date: Wednesday, January 04, 2012

Sheet 20 of 103

PCH(5/9)

USB2.0 Table

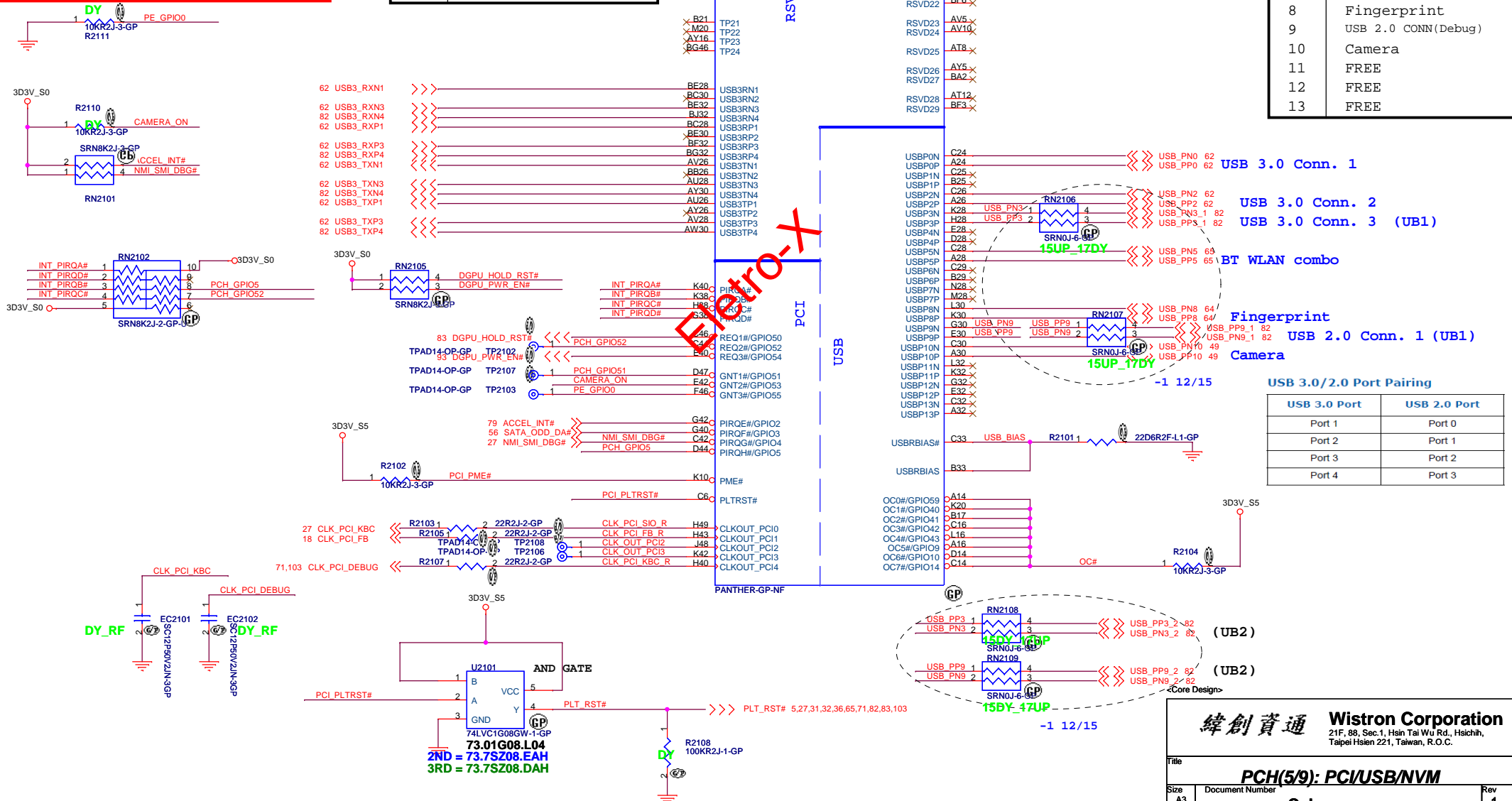
USB	
Pair	Device
0	USB 3.0 I/O CONN.
1	N/A
2	USB 3.0 I/O CONN.
3	USB 3.0 I/O CONN.
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 CONN(Debug)
10	Camera
11	FREE
12	FREE
13	FREE

USB3.0 Table

USB	
Pair	Device
1	I/O CONN. 1 LEFT_DOWN
2	FREE
3	I/O CONN. 2 LEFT_UP
4	I/O CONN. 3 RIGHT_UP

BOOT BIOS Strap

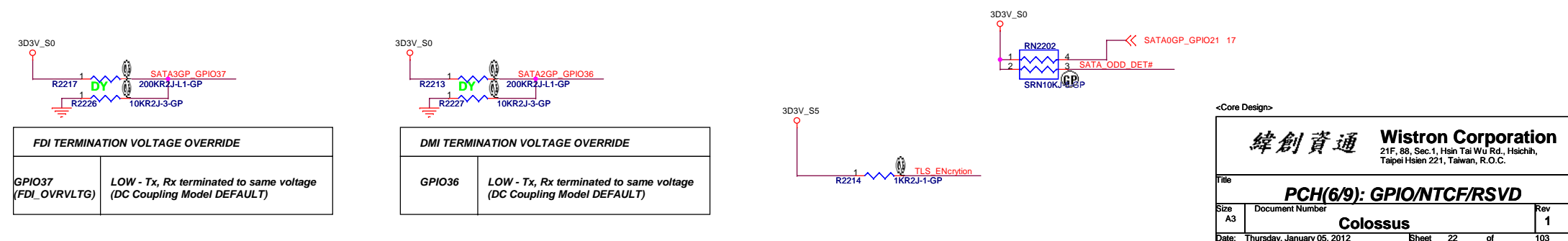
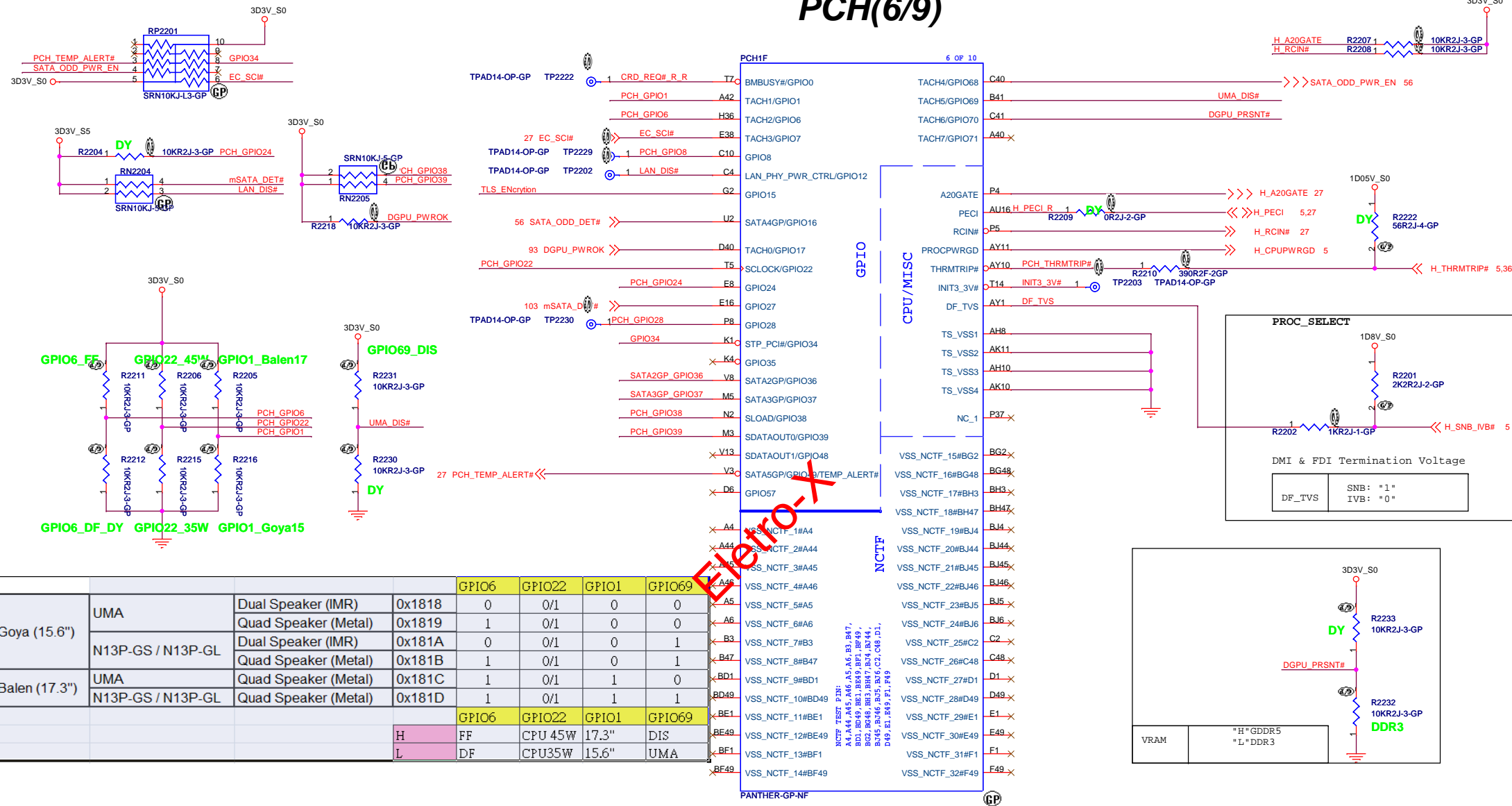
BOOT BIOS Strap		
GNT1#/ <u>GPIO51</u>	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



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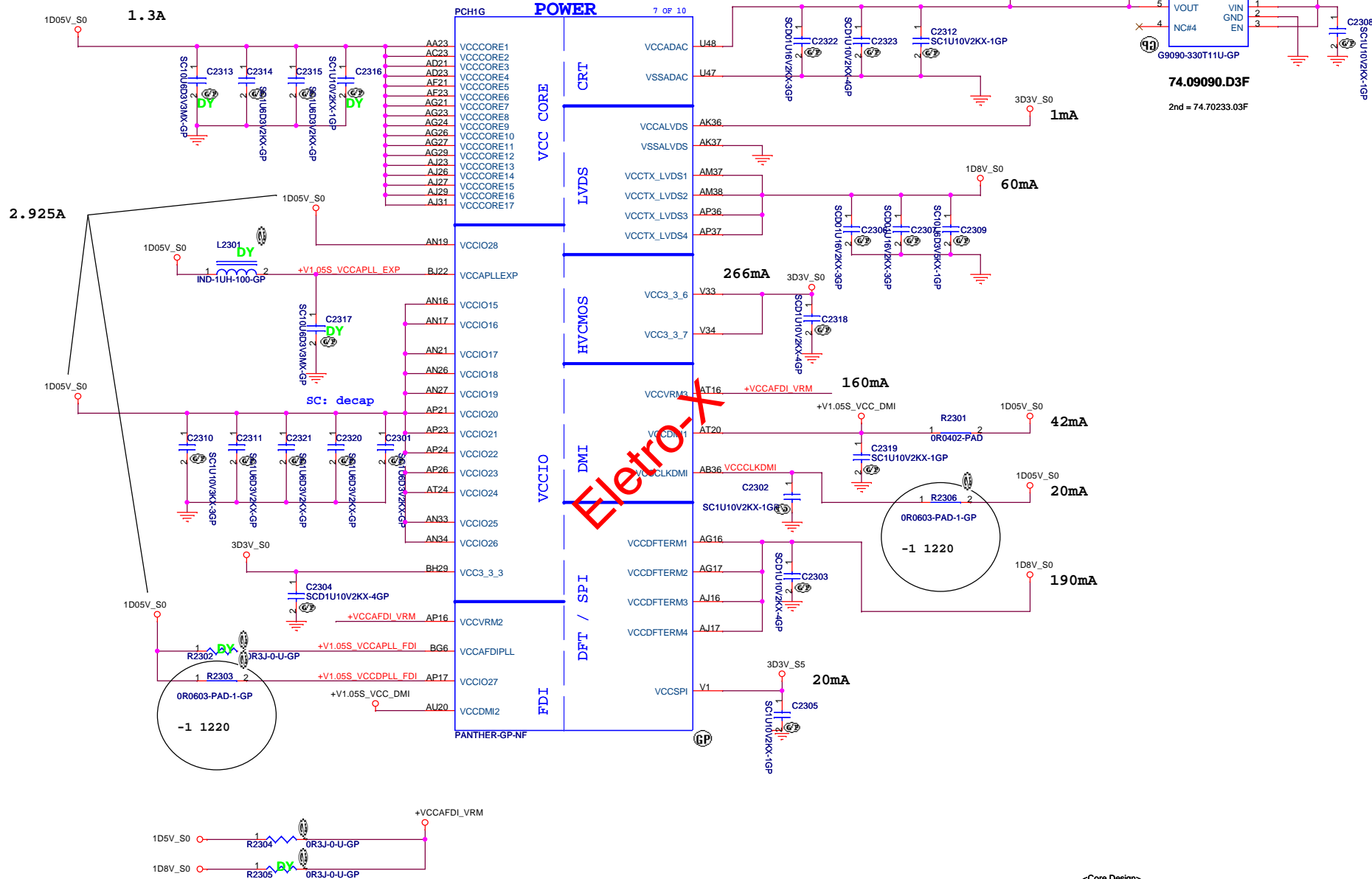
Title			
PCH(5/9): PCI/USB/NVM			
Size A3	Document Number		Rev
	Colossus		1
Date:	Wednesday, January 04, 2012	Sheet 21 of	103

PCH(6/9)



VCC_PCH: 6A

PCH(7/9)

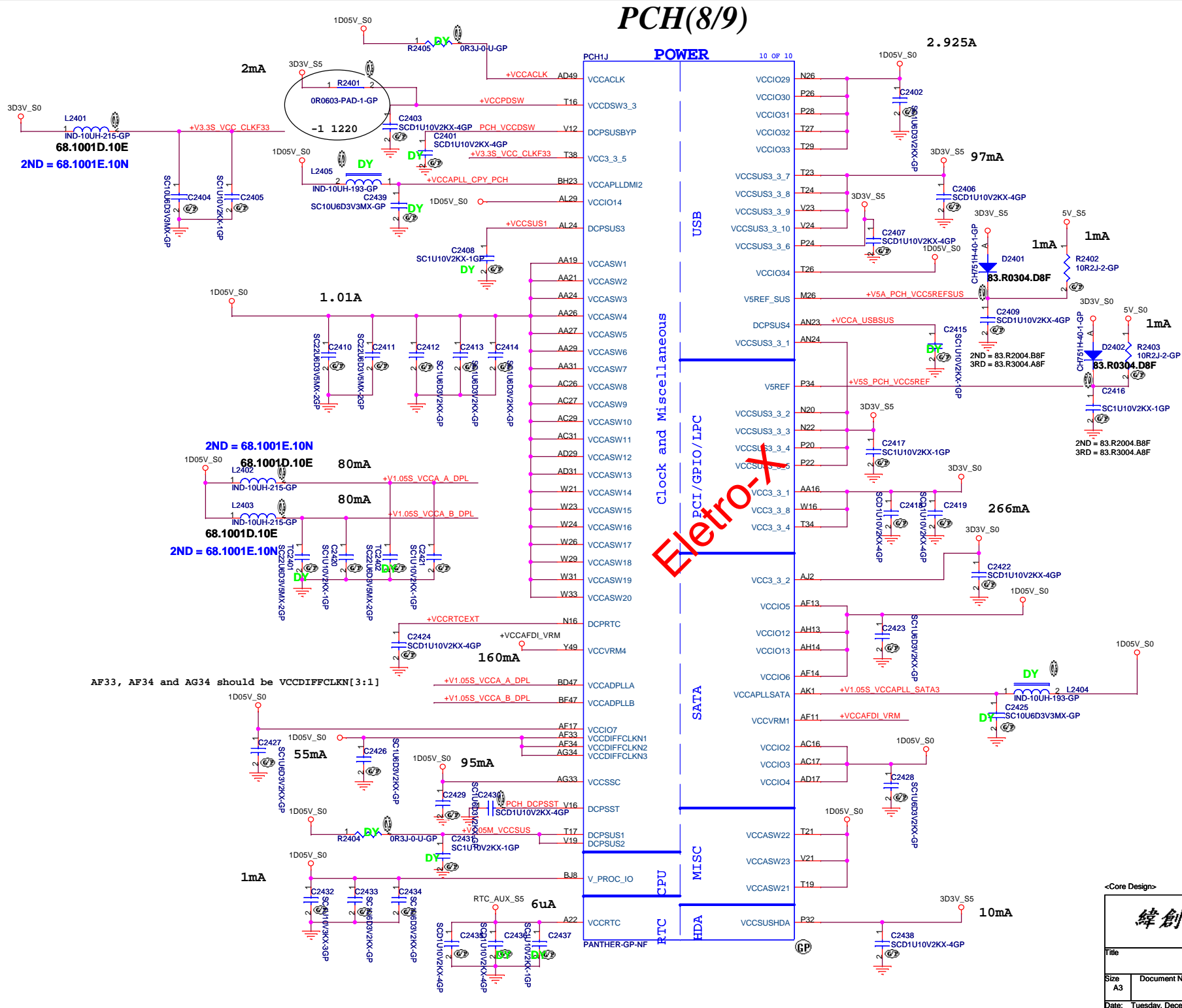


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Taipei Hsien 221, Taiwan, R.O.C.

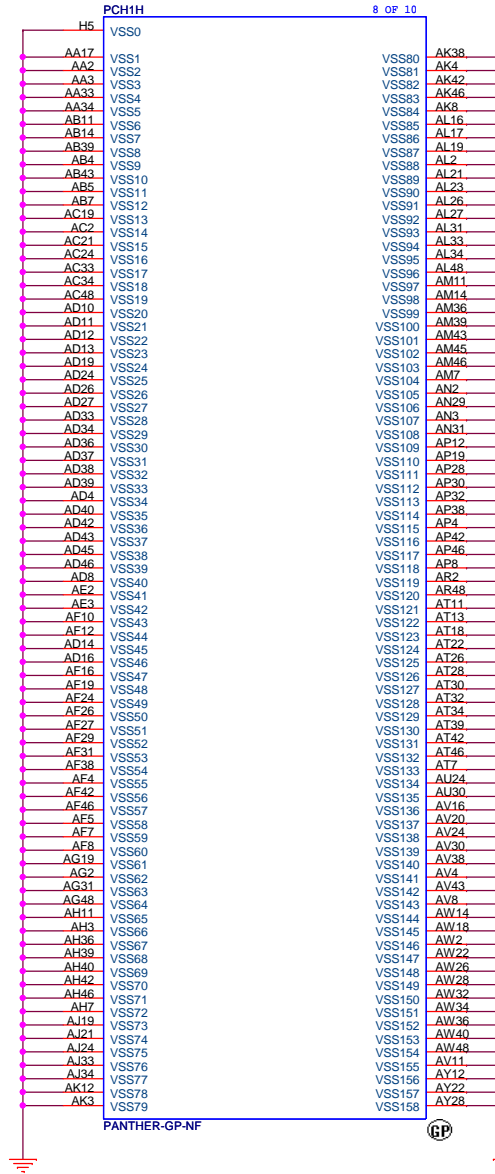
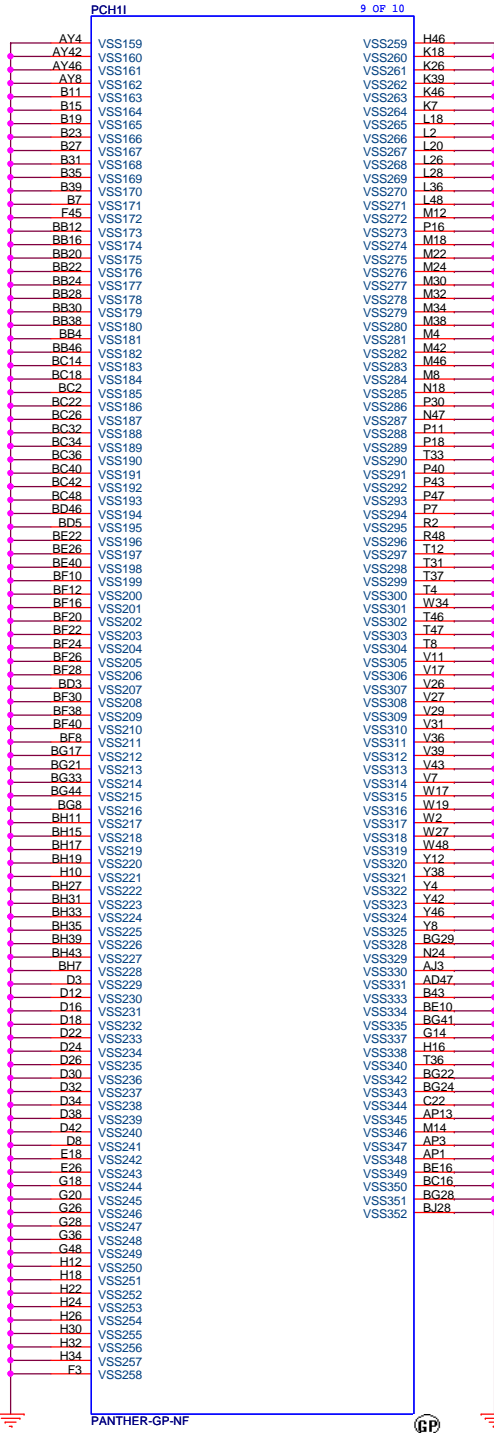
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Size	Document Number	Rev		
A3	Colossus	1		
Date:	Monday, December 26, 2011	Sheet	23	of 103

PCH(8/9)



PCH(9/9)

Eleto-X

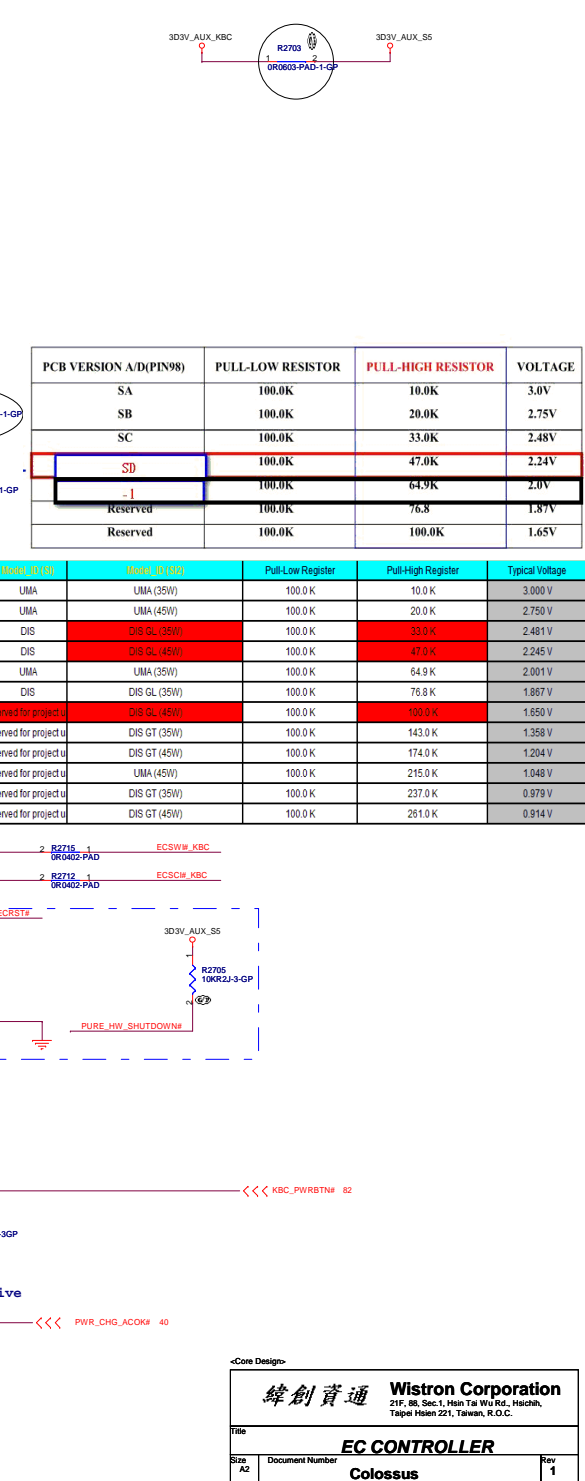
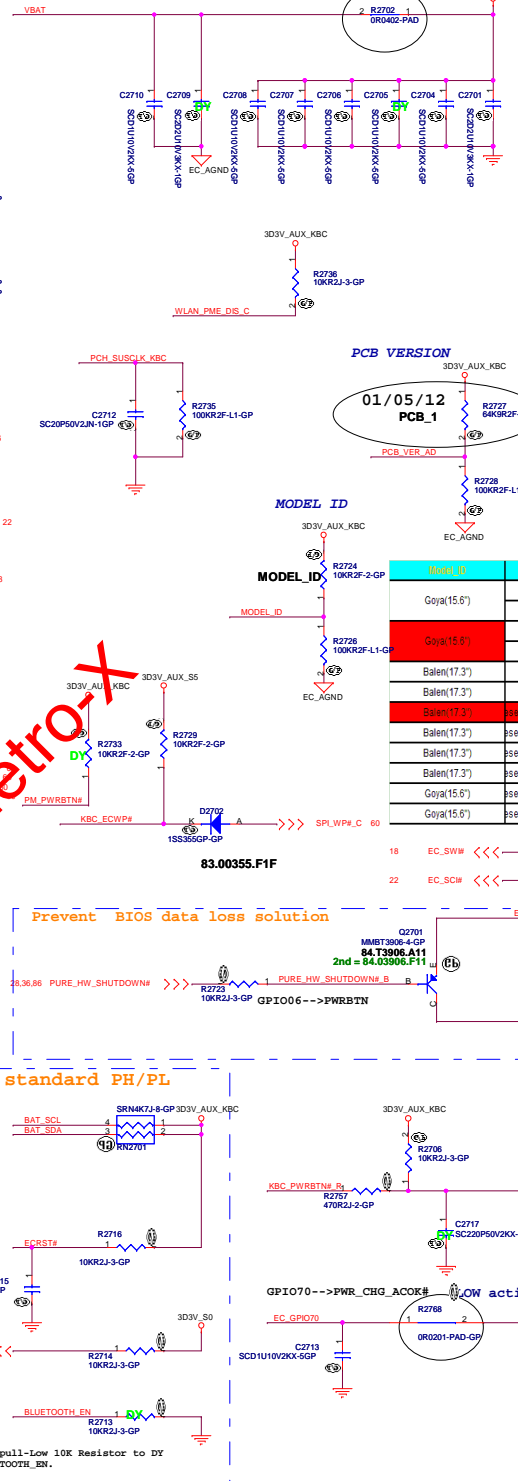
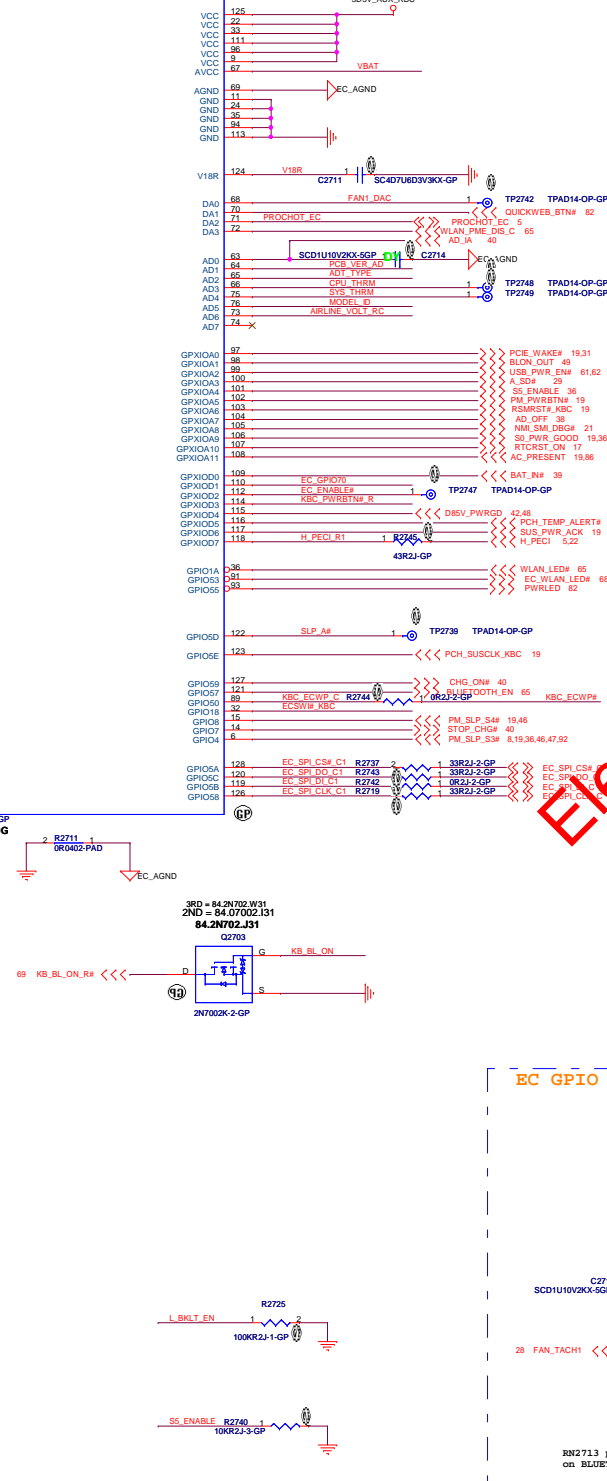
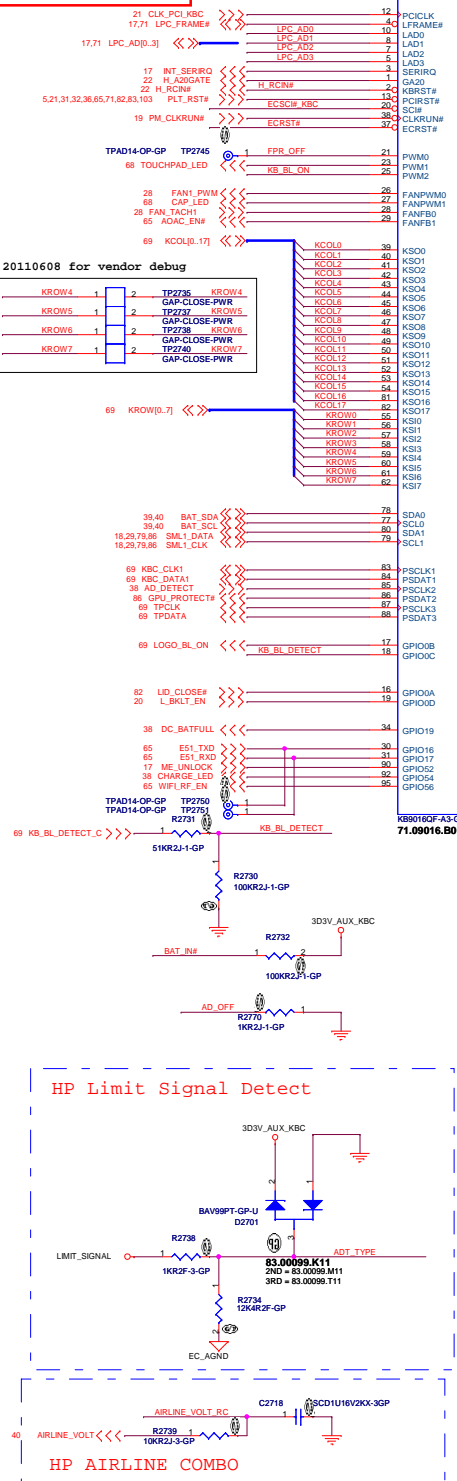


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Title			PCH(9/9): GND	
Size	Document Number	Rev		1
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SSID = KBC



PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-1	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V

Board ID	Model ID (1)	Model ID (2)	Pull-Low Register	Pull-High Register	Typical Voltage
Goya(15.6")	UMA	UMA (35V)	100.0 K	10.0 K	3.000 V
Goya(15.6")	UMA	UMA (45V)	100.0 K	20.0 K	2.750 V
Balen(17.3")	DIS	DIS GL (35V)	100.0 K	33.0 K	2.481 V
Balen(17.3")	DIS	DIS GL (45V)	100.0 K	47.0 K	2.245 V
Balen(17.3")	UMA	UMA (35V)	100.0 K	64.9 K	2.001 V
Balen(17.3")	DIS	DIS GL (35V)	100.0 K	76.8 K	1.887 V
Balen(17.3")	Reserved for project u	DIS GL (45V)	100.0 K	100.0 K	1.650 V
Balen(17.3")	Reserved for project u	DIS GT (35V)	100.0 K	143.0 K	1.358 V
Balen(17.3")	Reserved for project u	DIS GT (45V)	100.0 K	174.0 K	1.204 V
Balen(17.3")	Reserved for project u	UMA (45V)	100.0 K	215.0 K	1.048 V
Goya(15.6")	Reserved for project u	DIS GT (35V)	100.0 K	237.0 K	0.979 V
Goya(15.6")	Reserved for project u	DIS GT (45V)	100.0 K	261.0 K	0.914 V

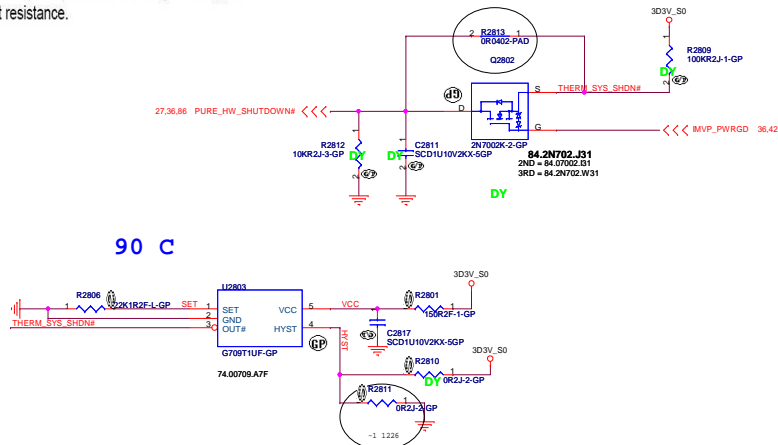
Electro-X

Prevent BIOS data loss solution

EC GPIO standard PH/PL

$$R_{SET}(k\Omega) = 0.0012T^2 - 0.9308T + 96.147$$

where T is the trip temperature in Centigrade. R_{SET} is the set-point resistance.



MT Global Mixed-mode Technology Inc.

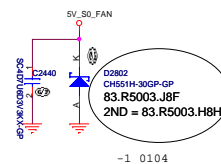
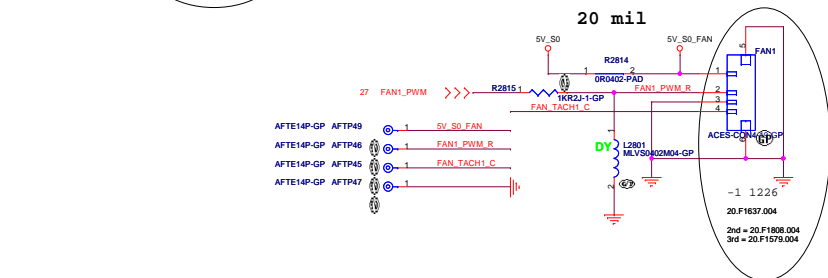
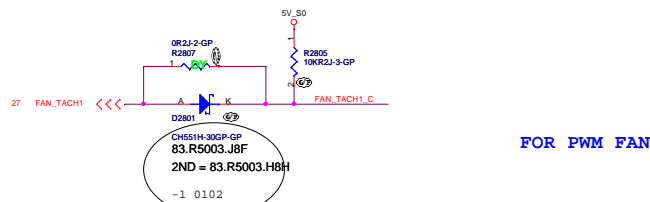
G709/G710

Pin Description

PIN	NAME	FUNCTION
G709	G710	
1	1	SET
2	2	GND
3	3	OT
4	4	HYST
5	5	N.C.
6	6	VCC

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
HYST Input Threshold	V_{IH}		0.7 x V_{CC}	---	---	V
	V_{IL}		---	---	0.3 x V_{CC}	V

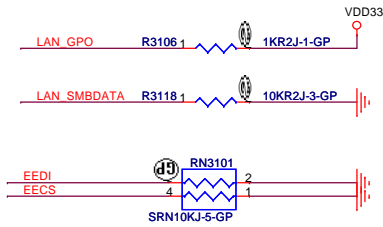
Eleto-X



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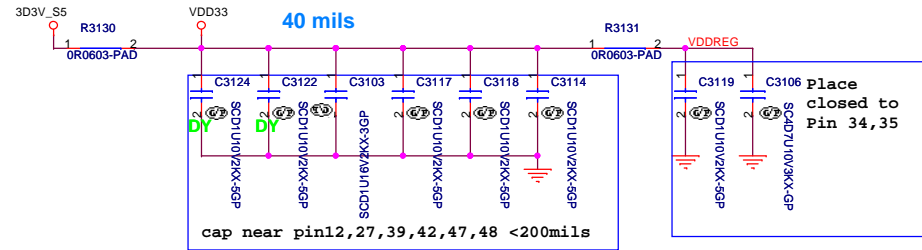
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichuan, Taipei Hsien 221, Taiwan, R.O.C.	
Thermal/FAN	
Title Size A2 Document Number Date: Wednesday, January 04, 2012	Rev 1

USE EFuse No ASF

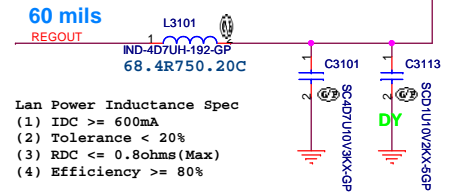
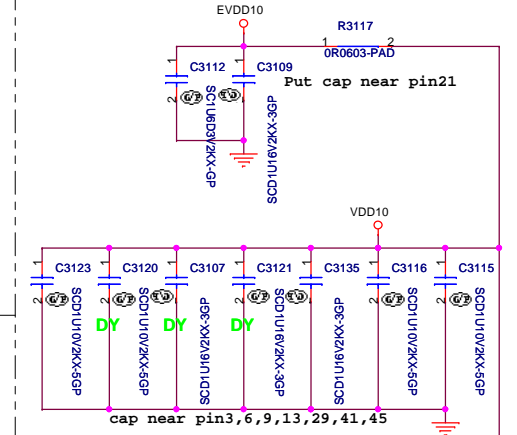


Avoid Leakage

LAN CHIP-RTL8111F



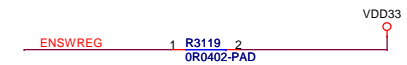
Regout power plane(1D05V)



Lan Power Inductance Spec
(1) IDC >= 600mA
(2) Tolerance < 20%
(3) RDC <= 0.8ohms(Max)
(4) Efficiency >= 80%

Put 4D7U L + 22U cap near pin36 <200mils
(2nd = 78.22610.81L)

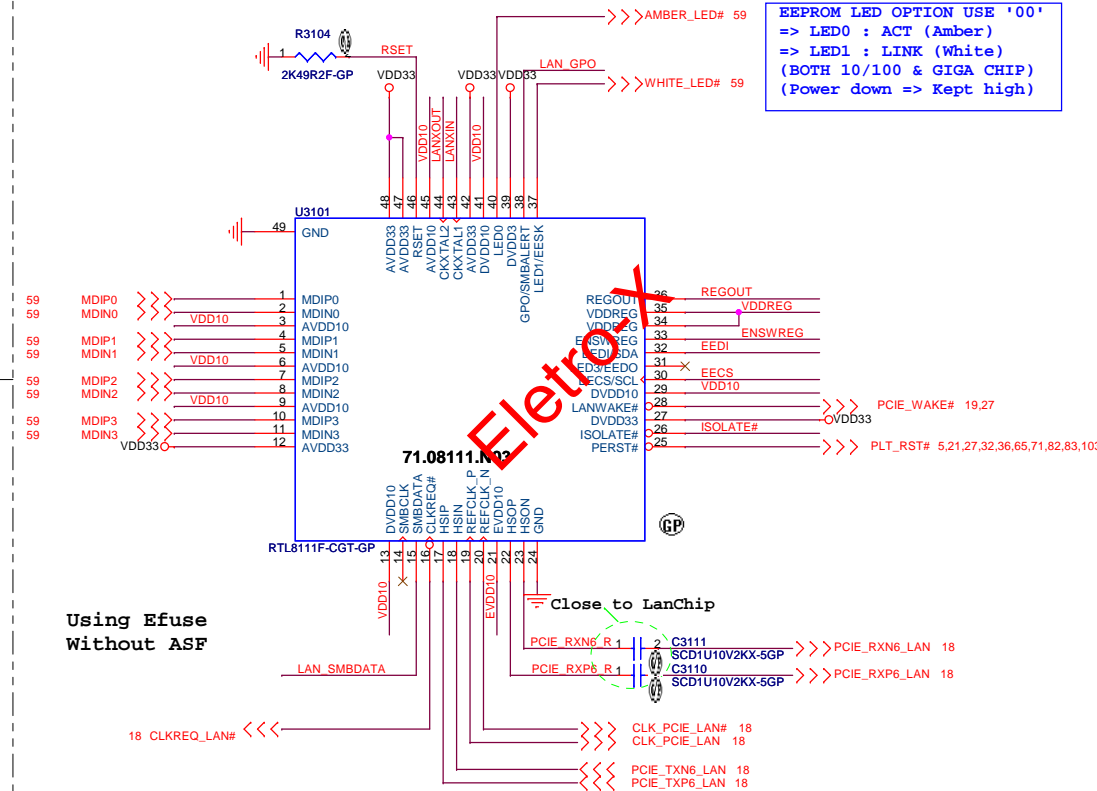
Regout Switch



ENSWREG (REGOUT 1D05V)
PH = Enable
PL = Disable

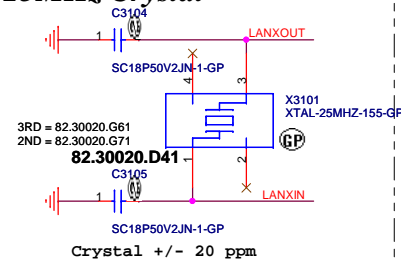
LanChip Power

+3.3V_LAN_S5 Rising time (10%~90%)
Spec >1ms and <100ms



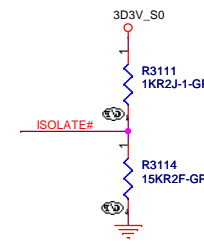
Using Efuse
Without ASF

25MHz Crystal



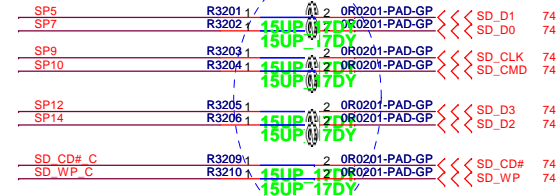
KBC Reserved Pin
Isolate# => Low , Isolate LanChip
GPO => EFuse Strap Pin

Isolate Strap Pin



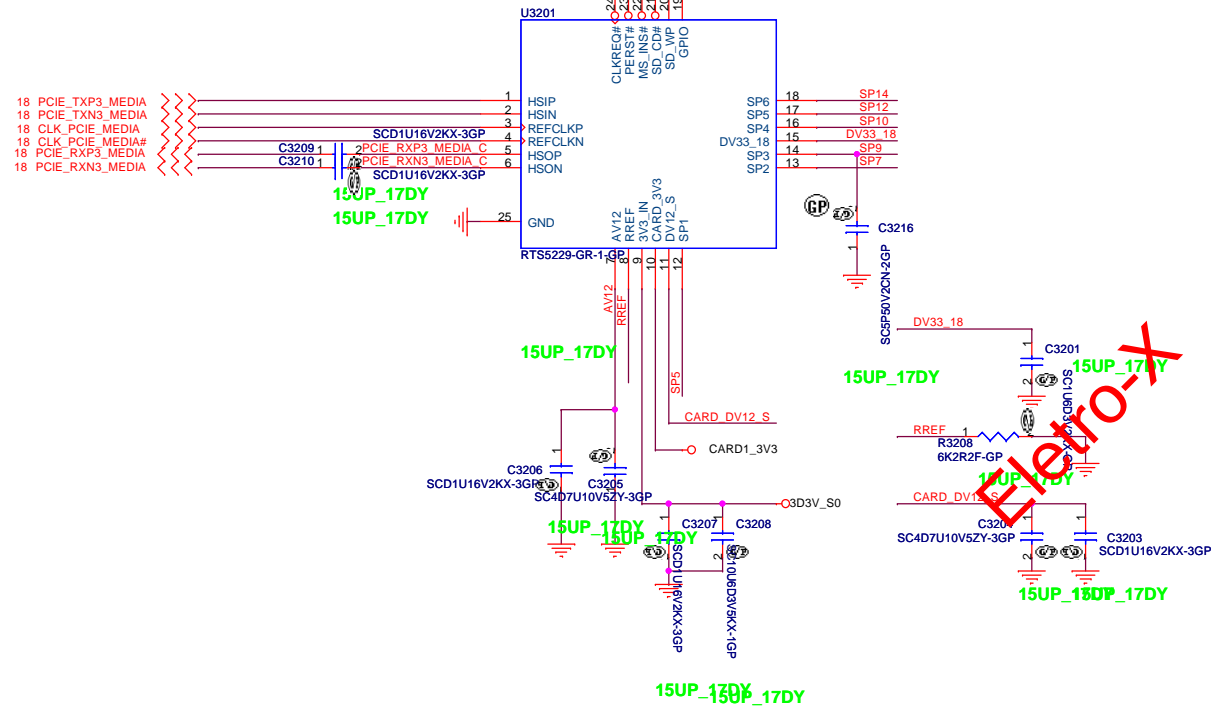
RTS5229

-1 12/15 0201 0 Ohm change to short pad



(RTS5229)U3201 closed near

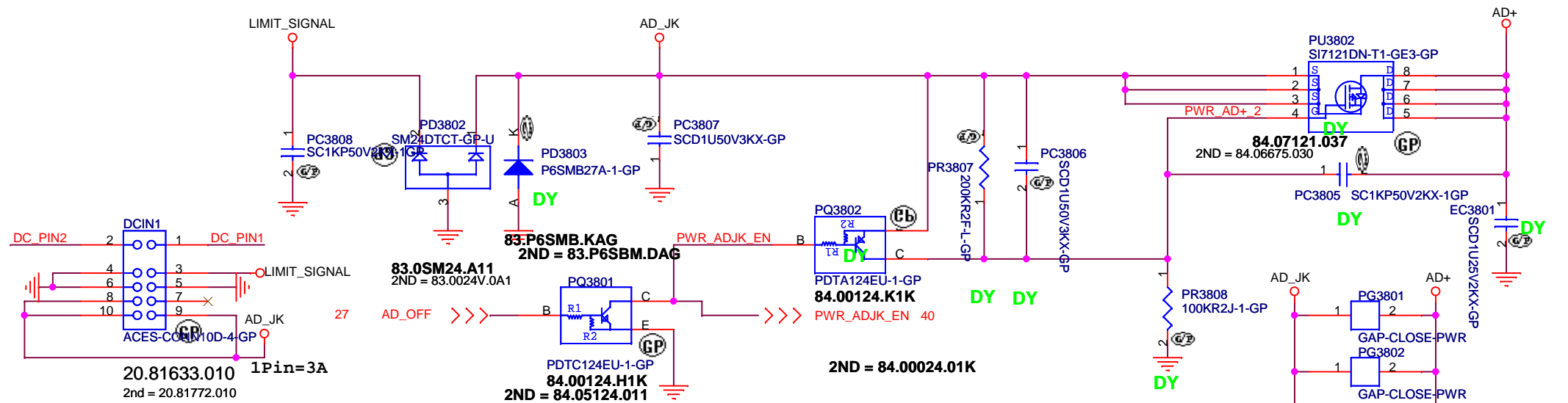
Vendor info update design issue



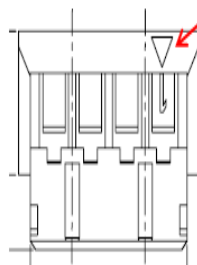
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Card Reader-RTS5229			
Size A3	Document Number Colossus		Rev 1
Date: Wednesday, January 04, 2012		Sheet 32 of 103	

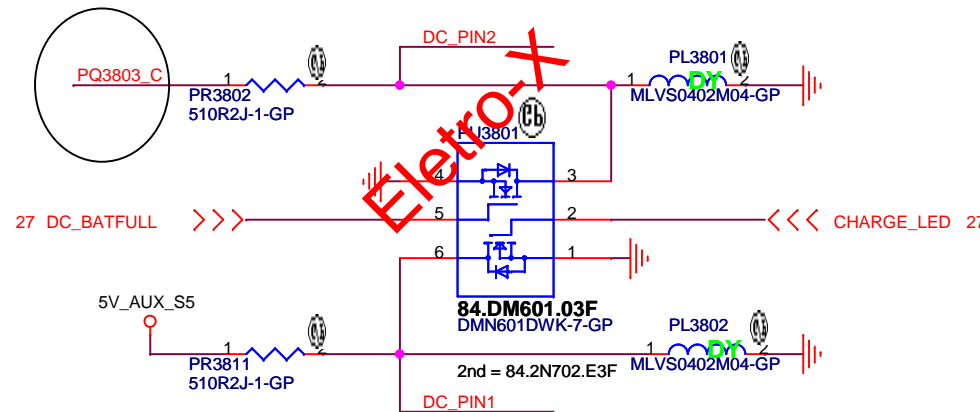
Adaptor in to generate DCBATOUT



Pin	Description	Wire color
Pin1	White LED	White
Pin2	Amber LED	Yellow
Pin3	ID	Brown
Pin4	GND	Black
Pin5	GND	Black
Pin6	GND	Black
Pin7	-	
Pin8	+VA	Red
Pin9	+VA	Red
Pin10	+VA	Red

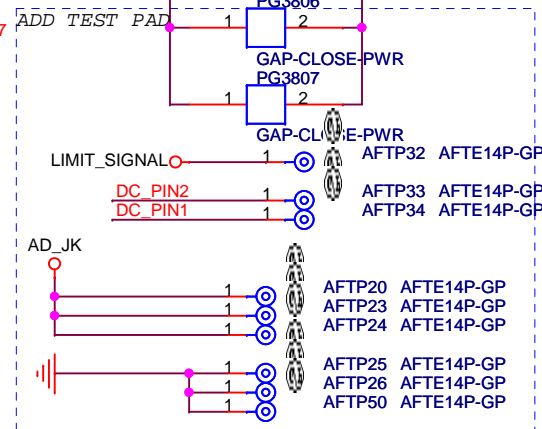
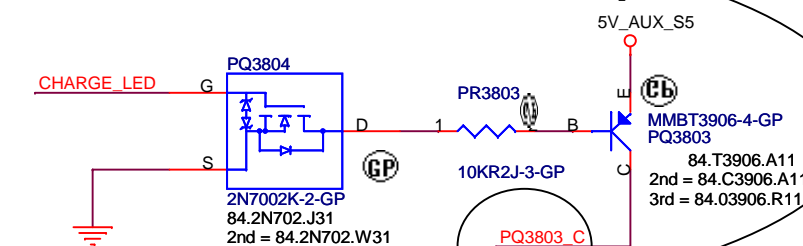
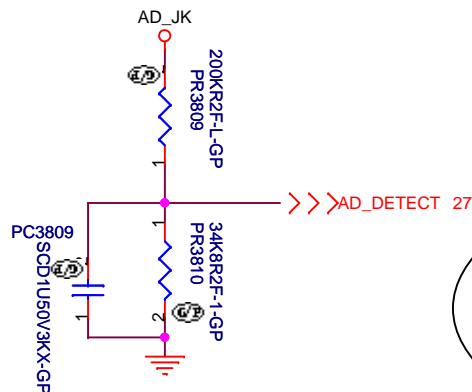


-1 1222 PR3802 to save 100mW when battery full.



AC Present = White
Standby = White pulsing
Charging = Amber
*LED's are off if no AC jack plugged in

-1 1222 PR3802 to save 100mW when battery full.



<Core Design>

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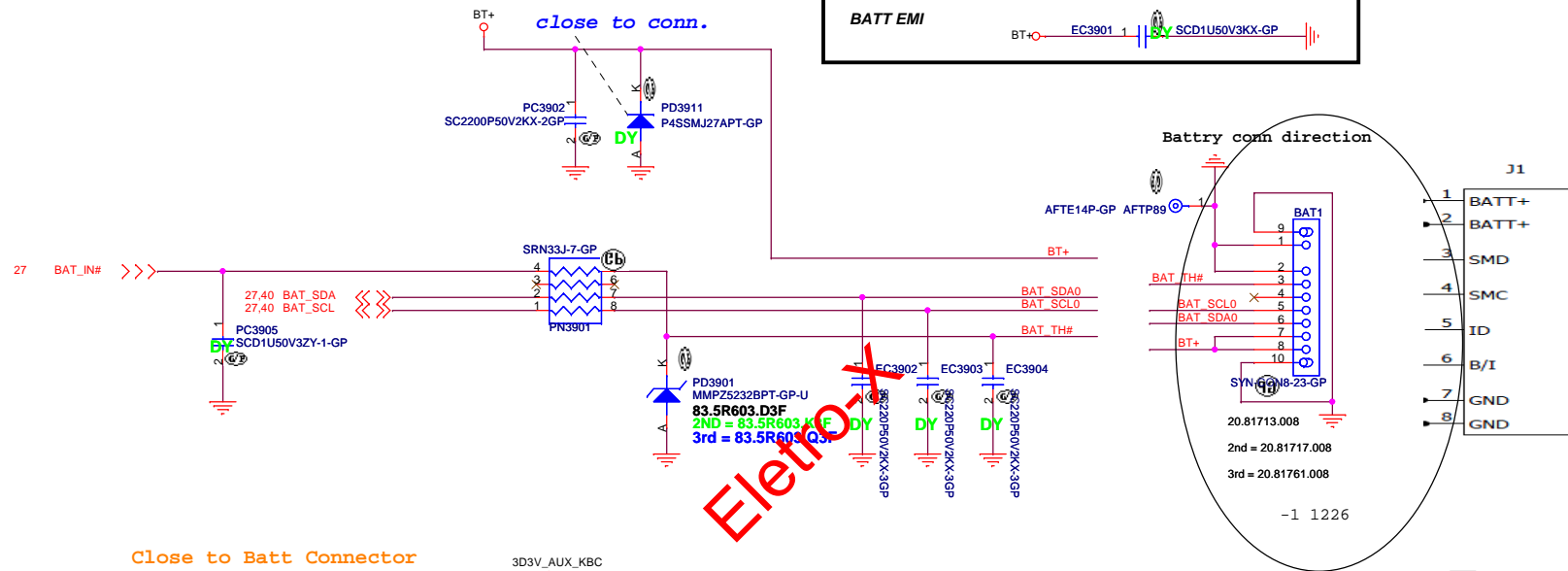
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title DCIN JACK

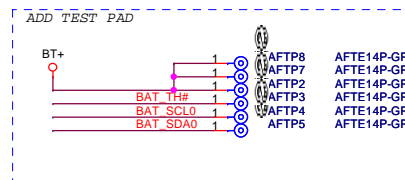
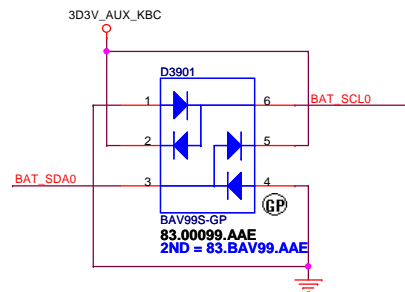
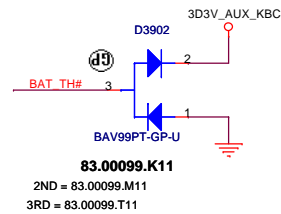
Size A4 Document Number Colossus Rev 1

Date: Wednesday, January 04, 2012 Sheet 38 of 103

BATT Connector



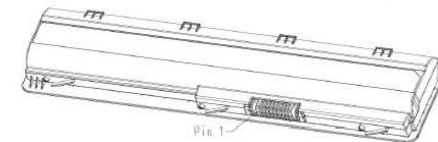
Close to Batt Connector



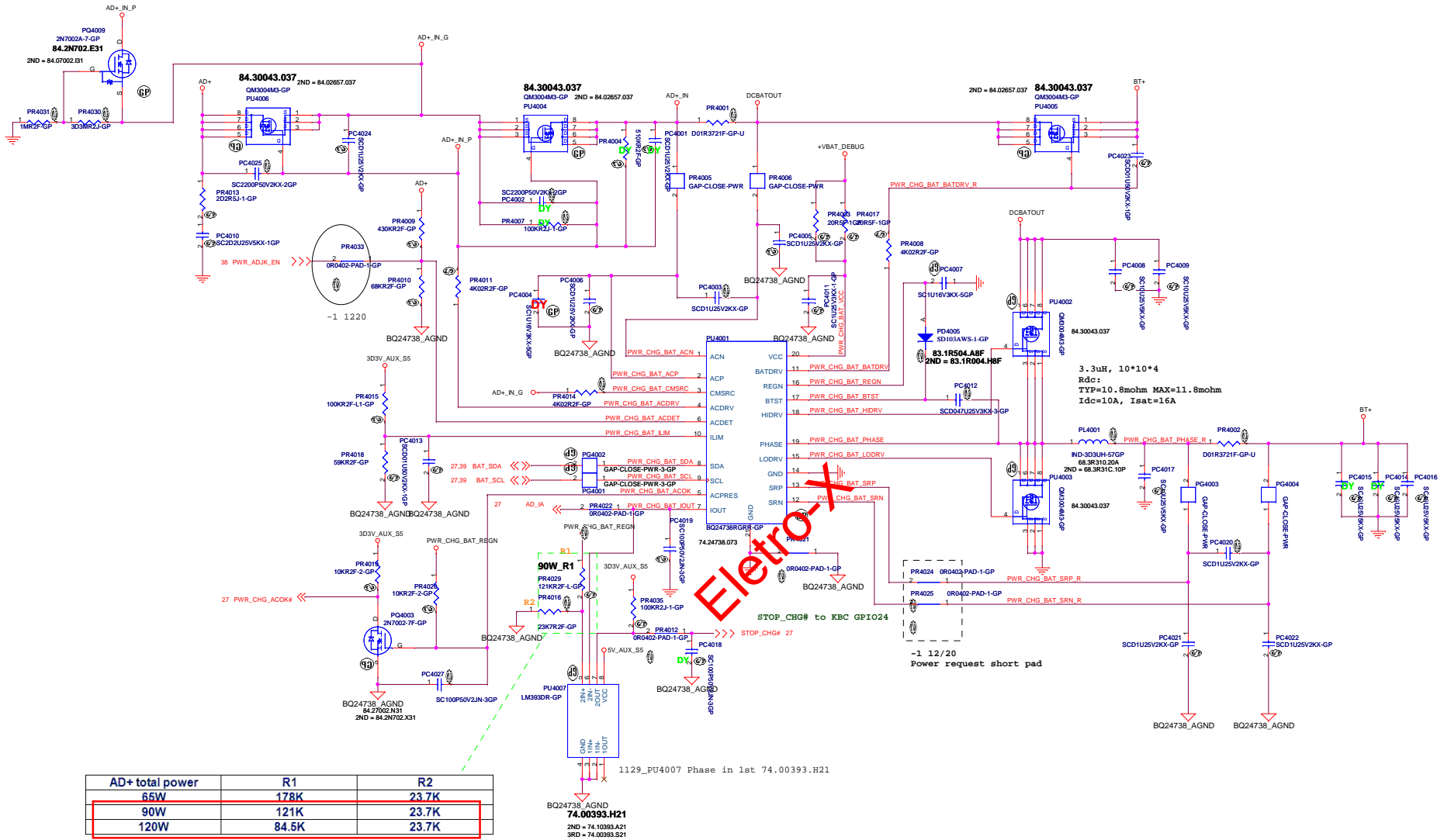
3. Interface

Connector ; 8pin
(Alltop C19029-10803-B, Foxconn BR0208C-B61H5-4H, Octek BTK-08ABEB)

Pin No.	Symbol	Description
1	BATT+	Batt+, Battery Positive Terminal
2	BATT+	Batt+, Battery Positive Terminal
3	SMD	SMBus data interface I/O pin
4	SMC	SMBus clock interface I/O pin
5	ID	Open
6	B/I	Connect to thermistor (103AT2 equivalent)
7	GND	Batt-, Battery Negative Terminal
8	GND	Batt-, Battery Negative Terminal

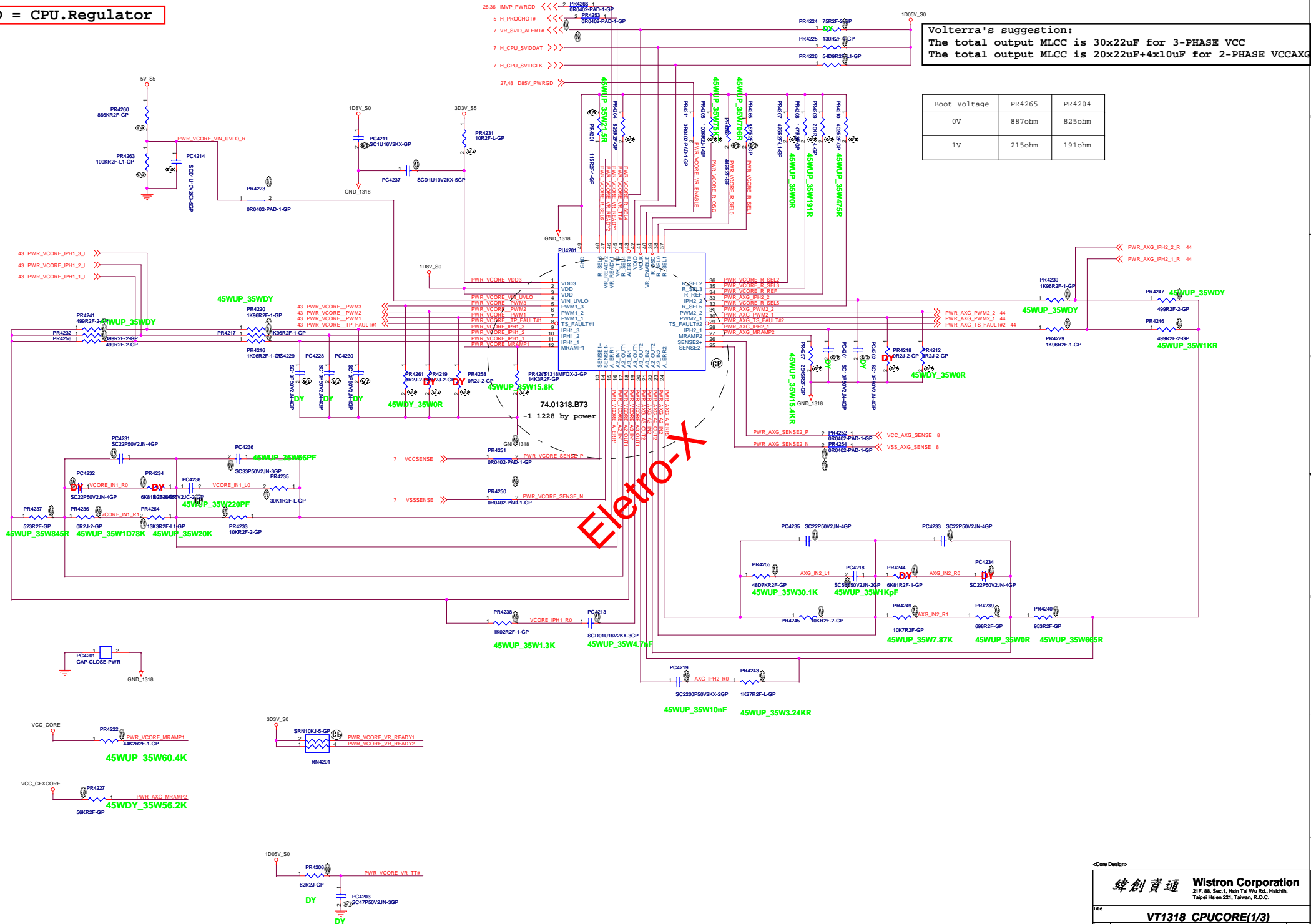


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<Core Design>

SSID = CPU.Regulator



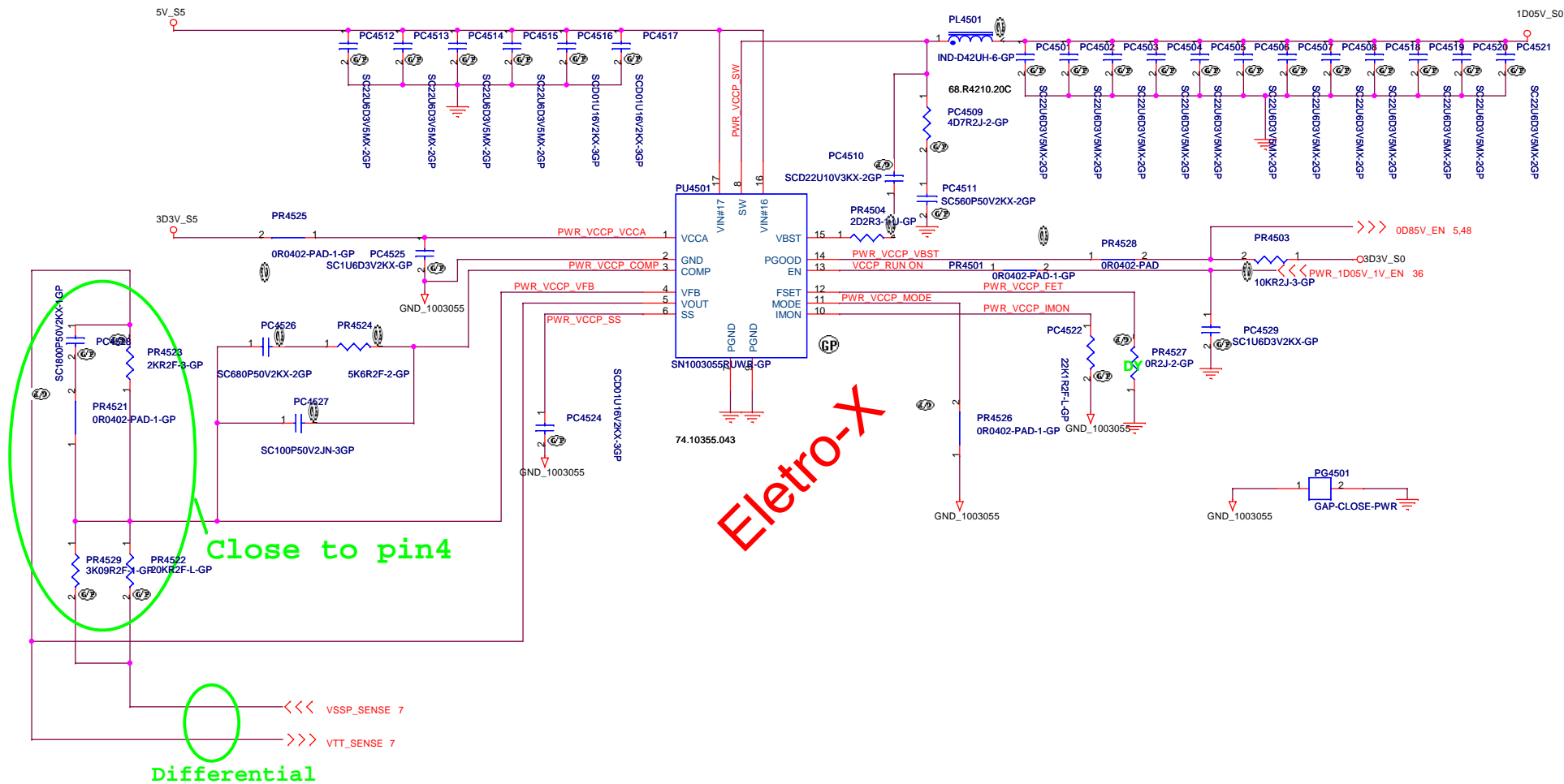
Volterra's suggestion:
The total output MLCC is 30x22uF for 3-PHASE VCC
The total output MLCC is 20x22uF+4x10uF for 2-PHASE VCCAXG

Boot Voltage	PR4265	PR4204
0V	887ohm	825ohm
1V	215ohm	191ohm

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File			VT1318 CPUCORE(1/3)
Size	Document Number	Rev	1
A2	Colossus		
Date: Wednesday, January 05, 2012			Sheet 42 of 103

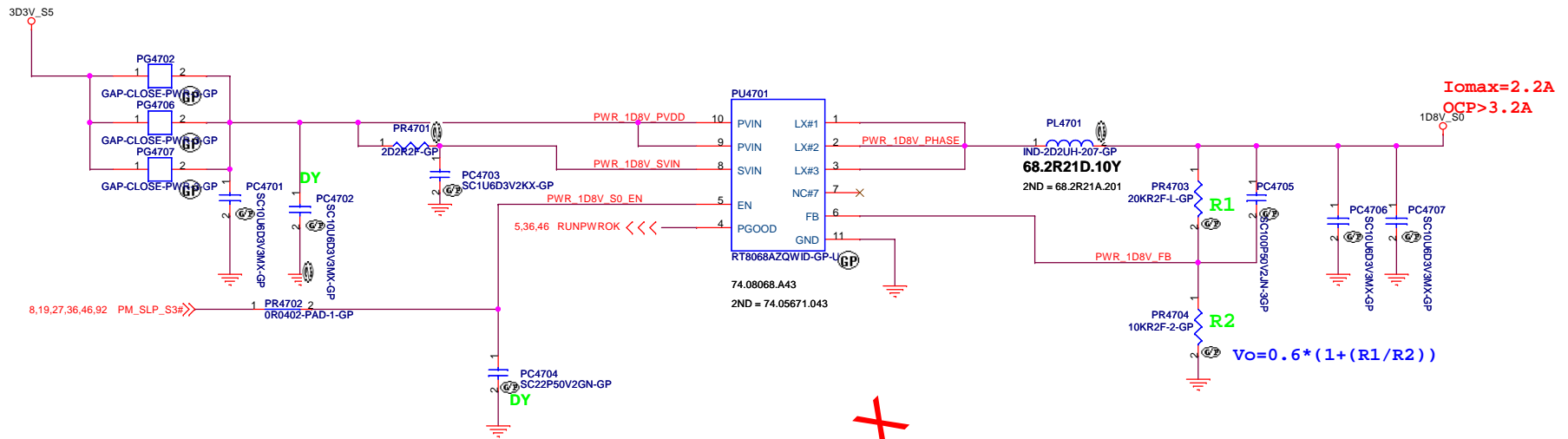


Iomax=16A
OCP>26A

<Variant Name>

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Title	
SN1003055RUWR	
Size	Document Number
A3	Colossus
Date: Wednesday, January 04, 2012	Sheet 45 of 103
Rev	1

RT8068A for 1D8V_S0



Eleto-X

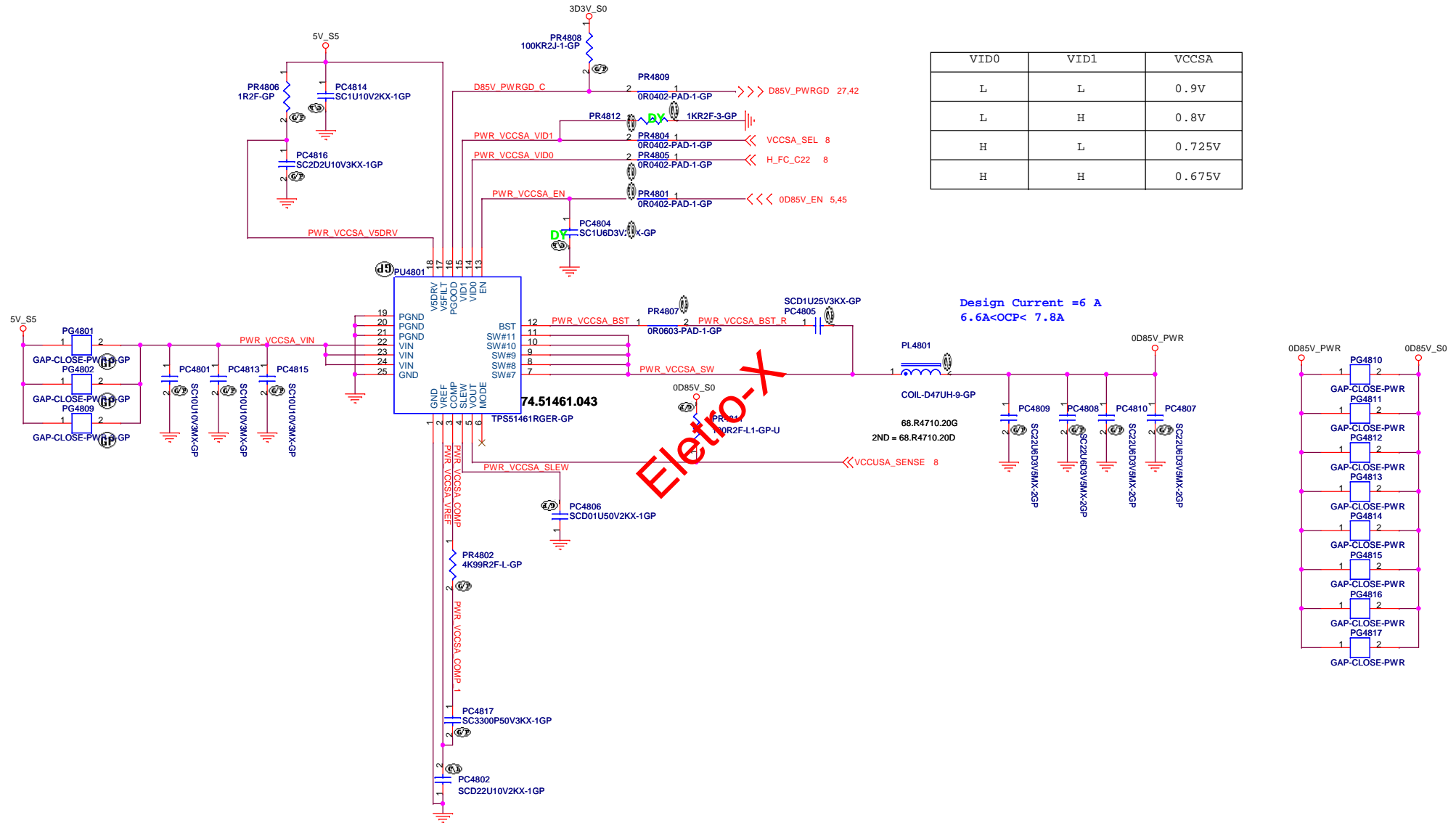
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Title			RT8068A 1D8V	
Size	Document Number	Rev		1
A3	Colossus			
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TPS51461 for VCCSA

VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

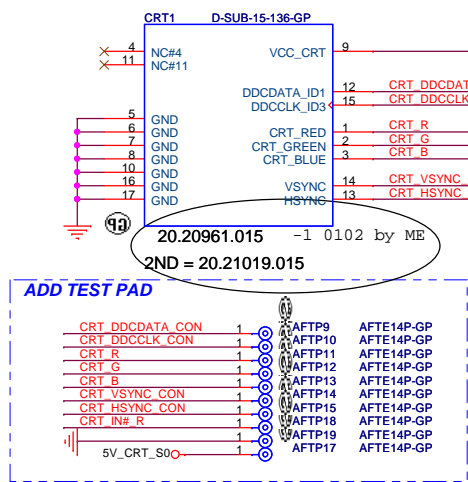


<Core Design>

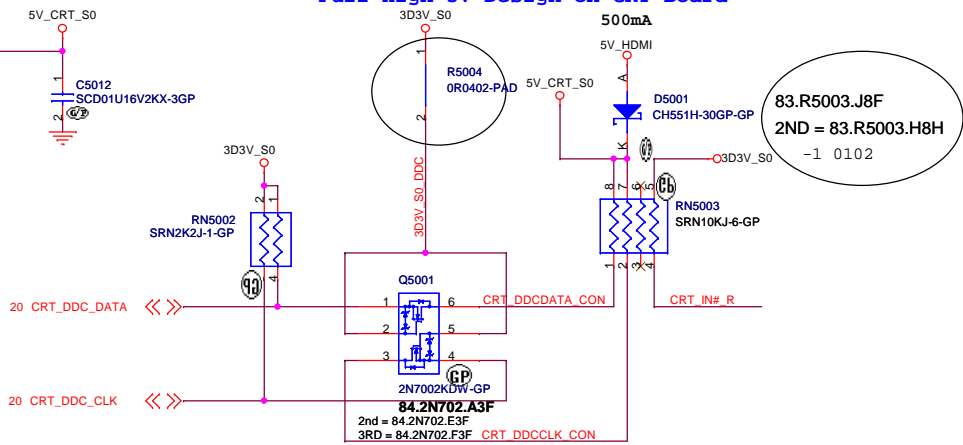
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
TPS51461 VCCSA		
Size	Document Number	Rev
A3	Colossus	1
Date:	Wednesday, January 04, 2012	Sheet 48 of 103

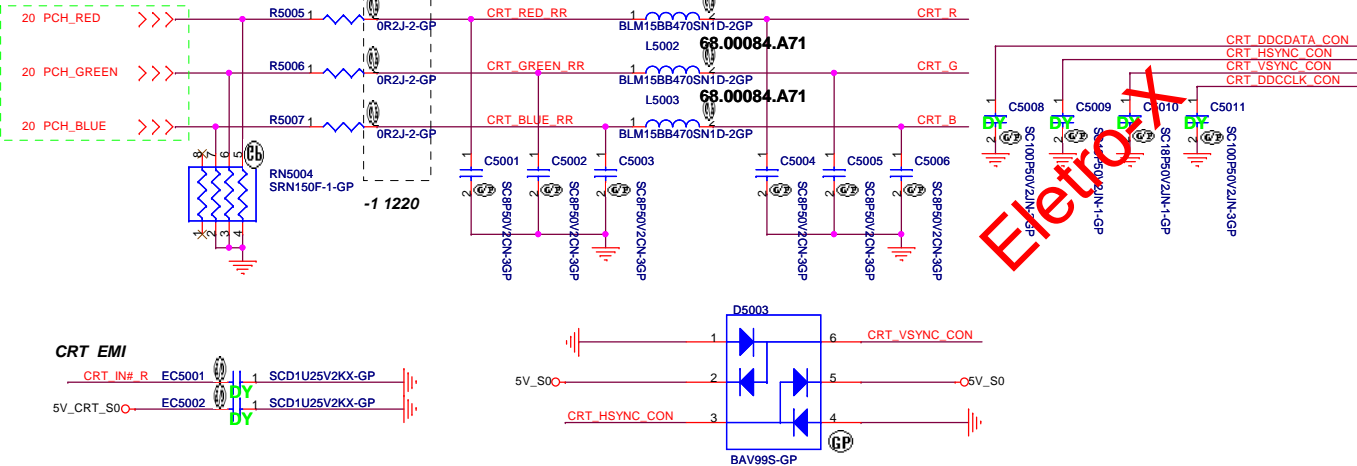
CRT Connector



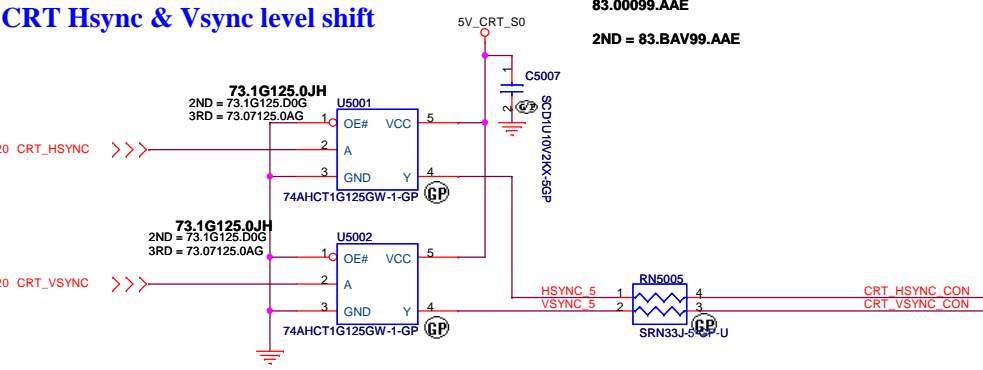
CRT DDCDATA & DDCCLK level shift
Pull High 5V Design on CRT Board



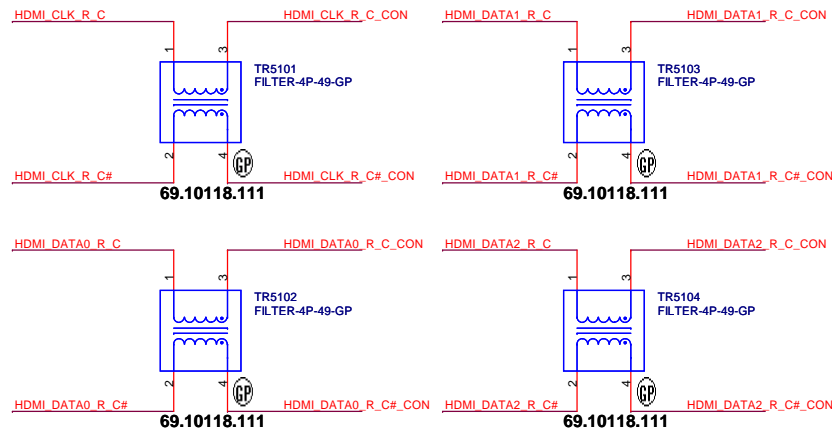
CRT RGB



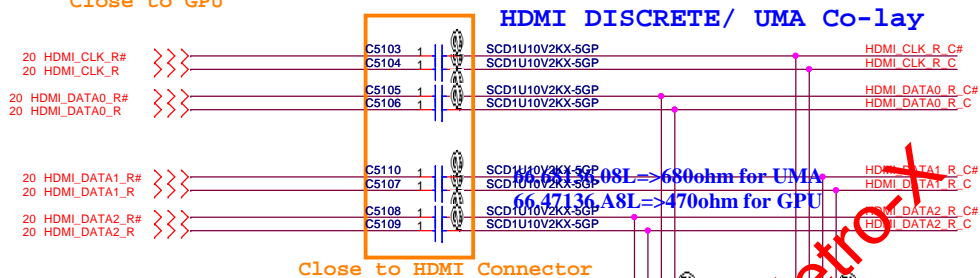
CRT Hsync & Vsync level shift



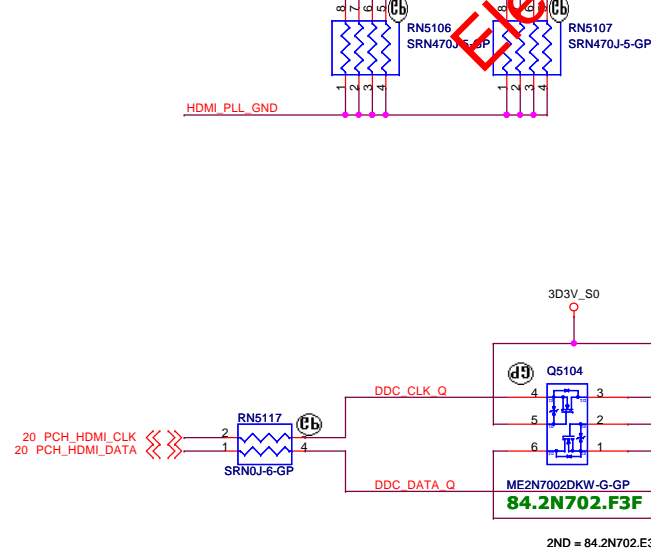
HDMI Level Shifter & CONNECTOR



Close to GPU



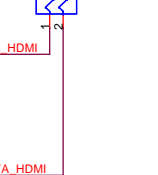
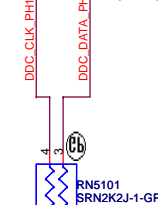
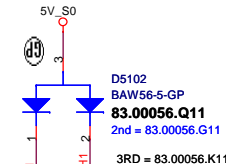
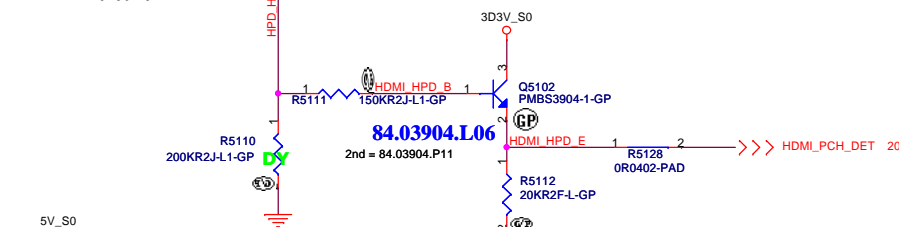
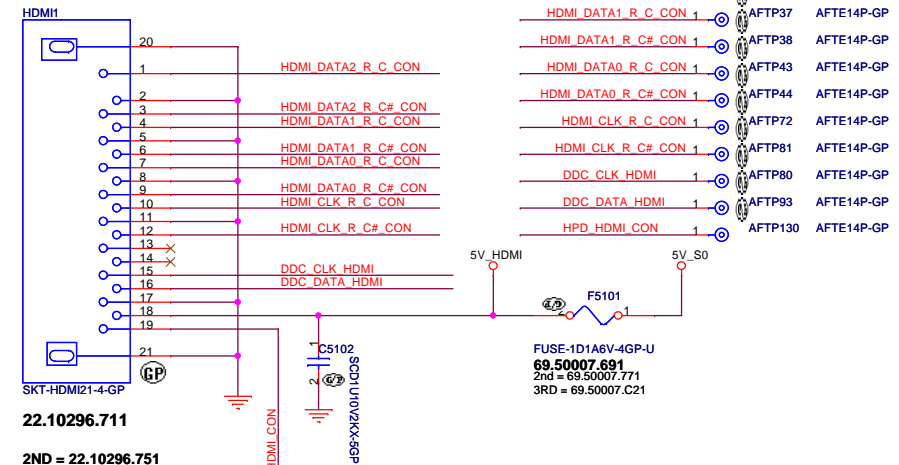
Close to HDMI Connector



Routing Guidelines:

CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

HDMI CONN



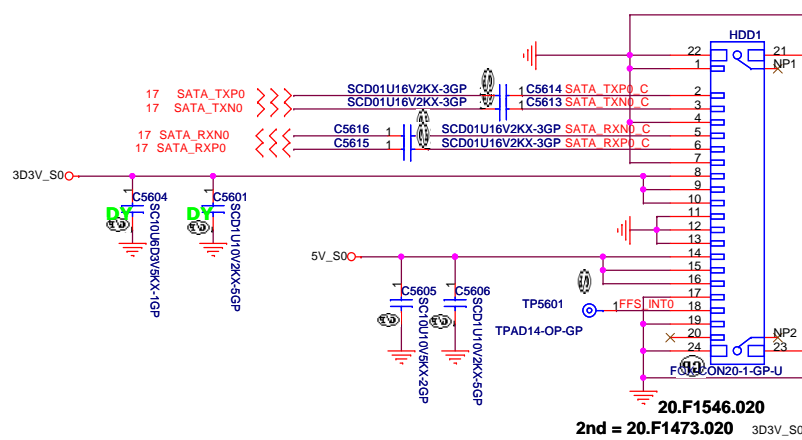
<Core Design>

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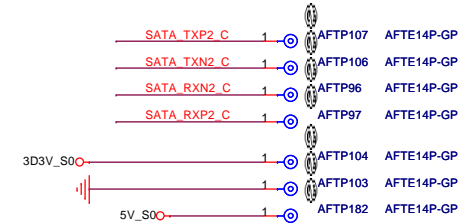
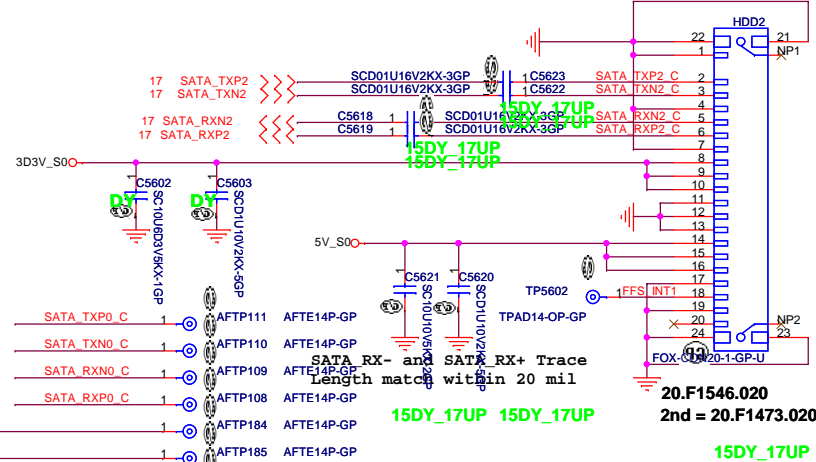
Title		
HDMI Level Shifter/Conn		
Size	Document Number	Rev
A3	Colossus	1
Date: Wednesday, January 04, 2012 Sheet 51 of 103		

SATA HDD1 Connector

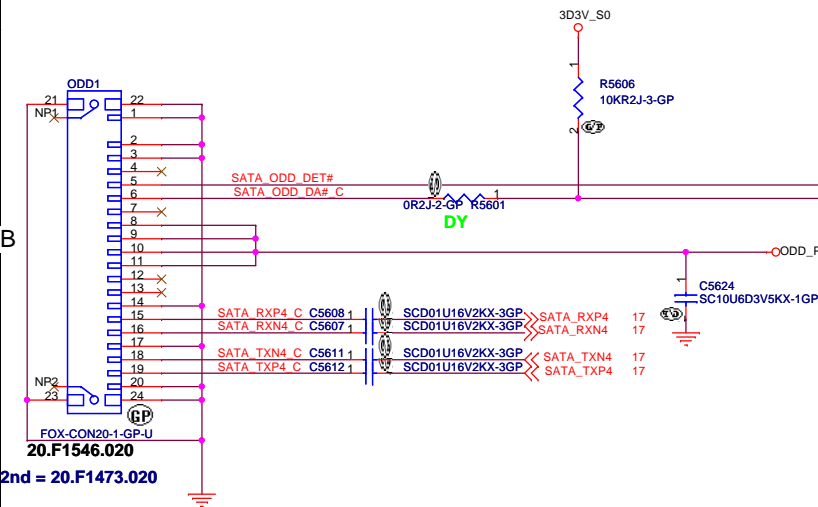
CHECK HDD conn model pin define_ME wire



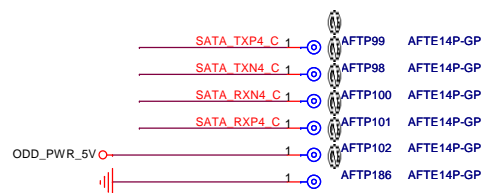
SATA HDD2 Connector



ODD Connector

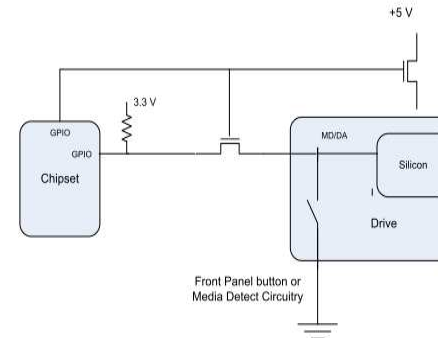


SUPPORT ZERO SATA ODD

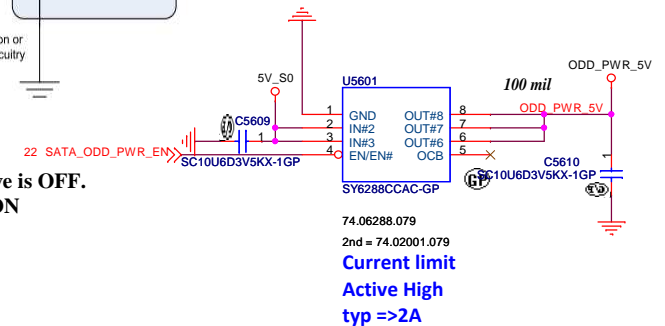


When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

Q5601
ME2N7002DKW-G-GP
84.2N702.F3F
2ND = 84.2N702.E3F

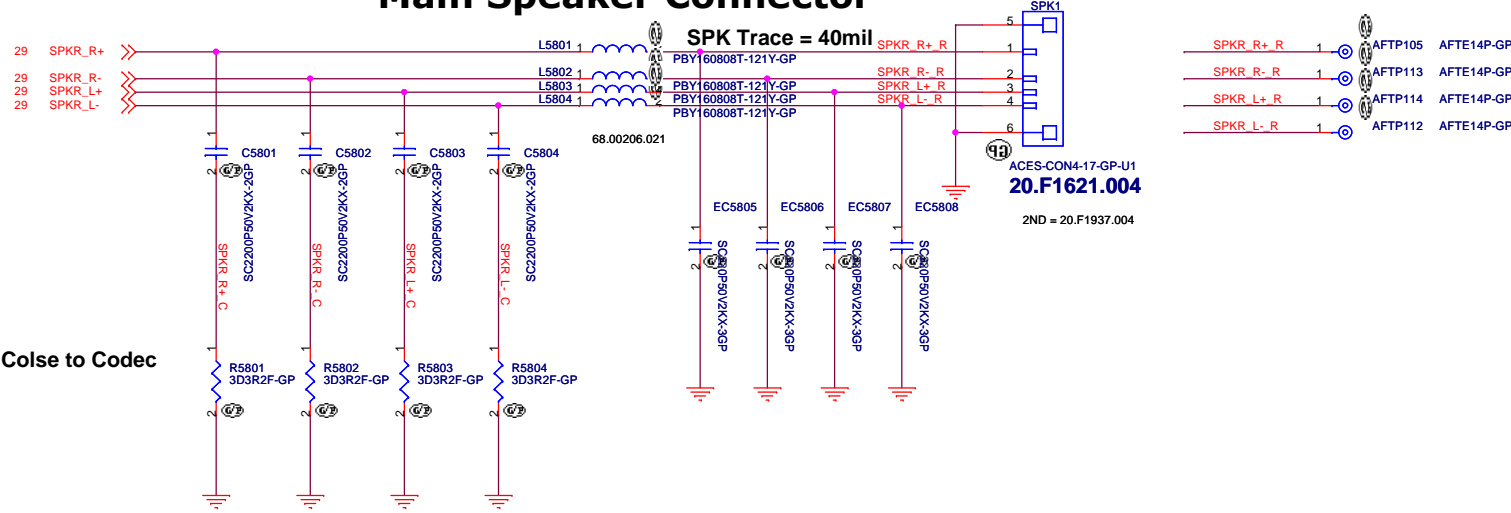


SATA Zero Power ODD



<Core Design>

Main Speaker Connector

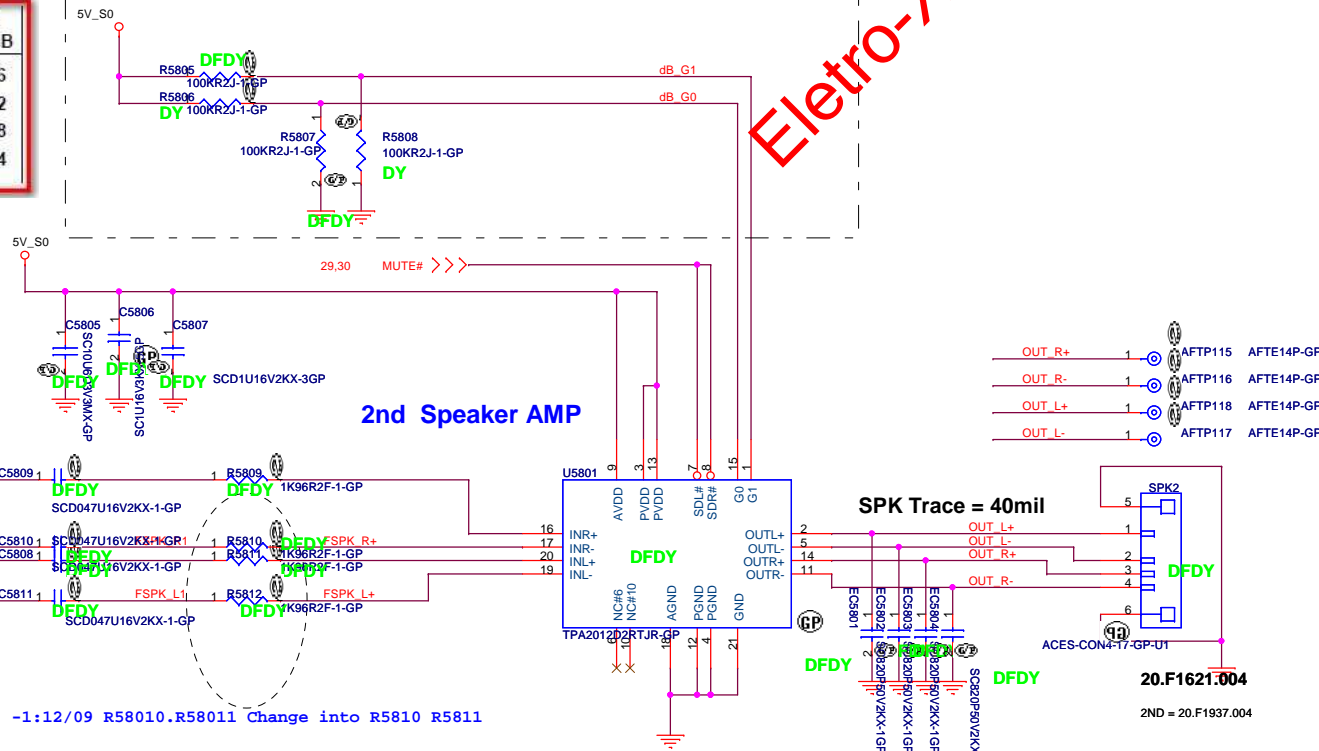


Colse to Codec

GAIN 18dB

G1	G0	V/V	Gain
0	0	2	6
0	1	4	12
1	0	8	18
1	1	16	24

2ND Speaker Connector



GND near by CODEC

-1:12/09 R58010.R58011 Change into R5810 R5811

<Core Design>

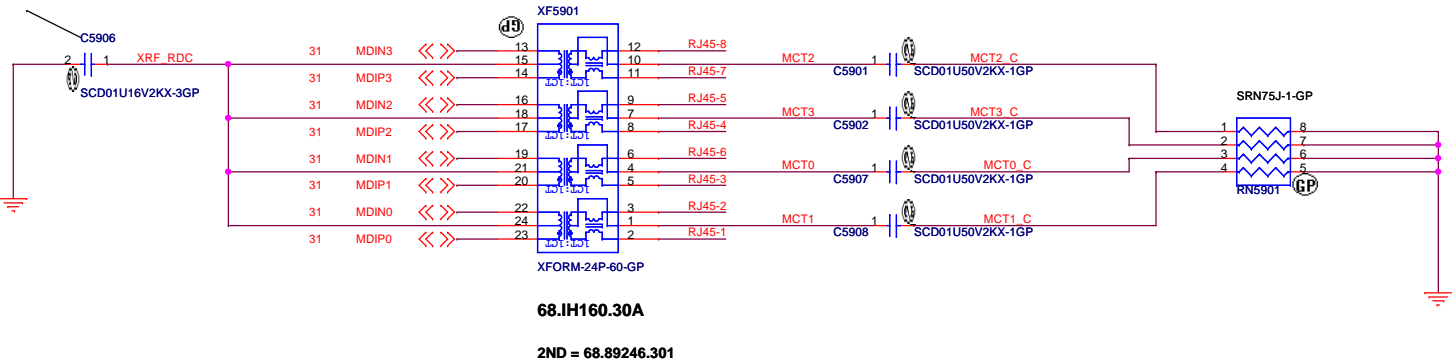
緯創資通 Wistron Corporation
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Title		
SPEAKER CONN		
Size	Document Number	Rev
A3	Colossus	1
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White LED for connectivity and Amber LED for activity located on RJ-45 connector

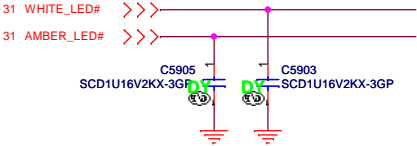
close to XF1

close to XF1

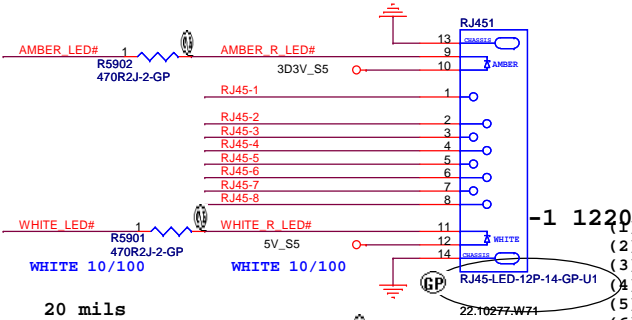


Eleto-X

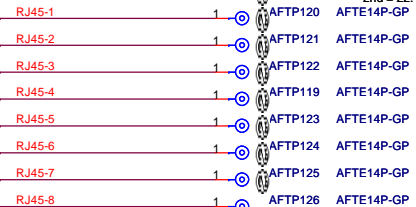
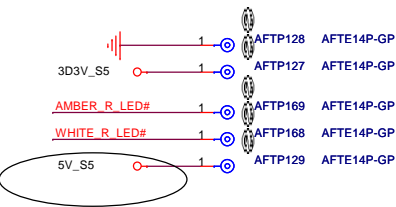
AMBER = LAN ACK



RJ451



- 20 mils
- 2nd = 22.10177.N81
- (1) route on bottom as differential pairs.
 - (2) Tx+/Tx- are pairs. Rx+/Rx- are pairs.
 - (3) No vias, No 90 degree bends.
 - (4) pairs must be equal lengths.
 - (5) 6mil trace width, 12mil separation.
 - (6) 36mil between pairs and any other trace.
 - (7) Must not cross ground moat, except RJ-45 moat.

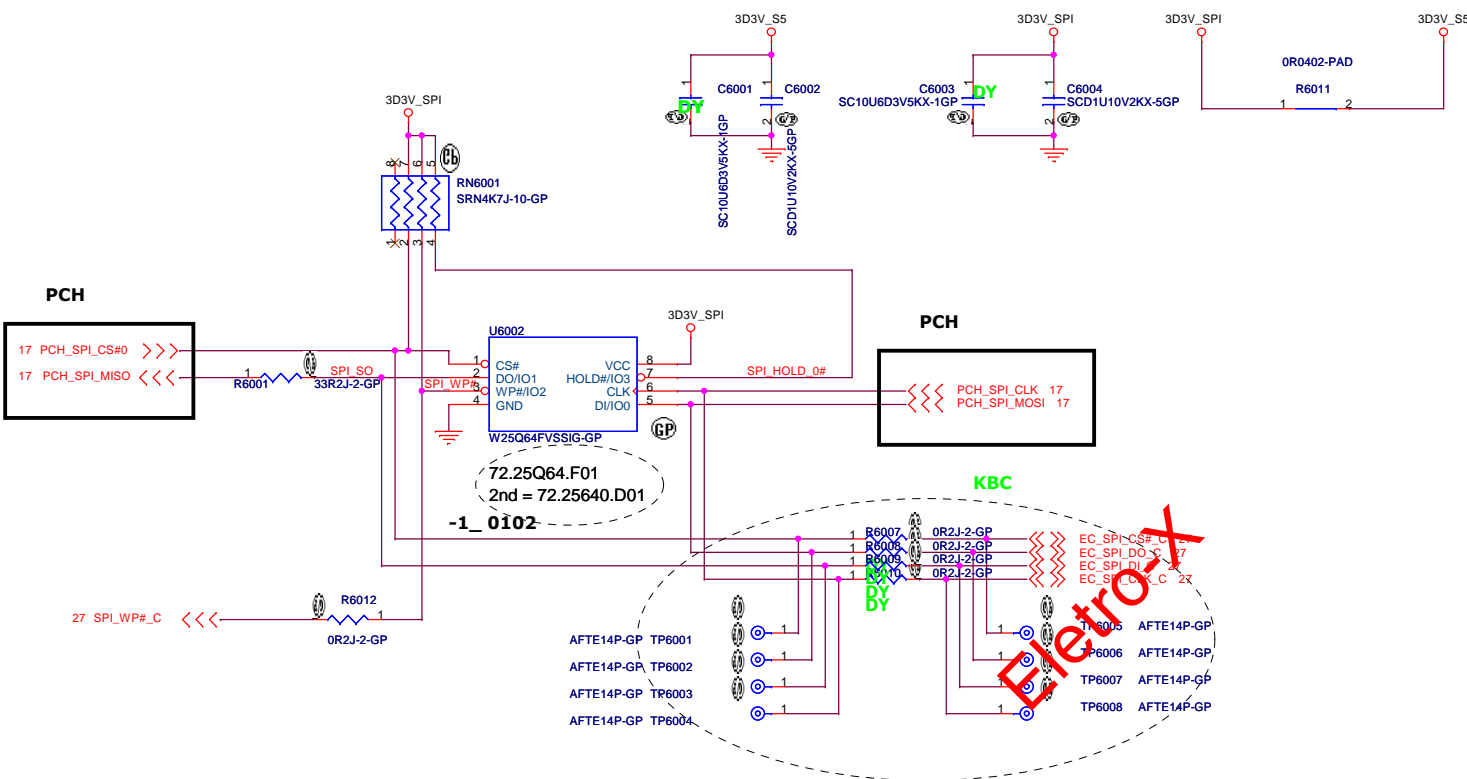


SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH & KBC

Notes:

The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil



- 1 1223 Reversed TP6001~TP6008 / R6007~R6010 is DY
1, 測試點請使用14mil, 測試之間距離75mil以上。
2, 測試點必須在Top層。

<Core Design>

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Title

Flash

Size
A3

Document Number

Colossus

Rev
1

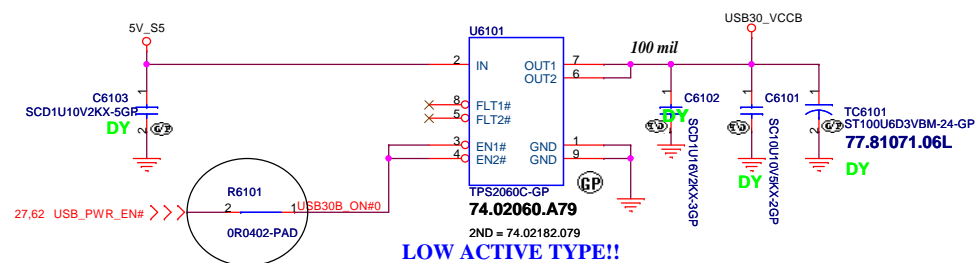
Date: Wednesday, January 04, 2012

Sheet 60 of 103

RESERVED USB 2.0/3.0 BD

SSID = USB

Power switcher Low active



Eletro-X

<Core Design>

緯創資通

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Title

USB Power SW USB IO

Size
A3

Document Number

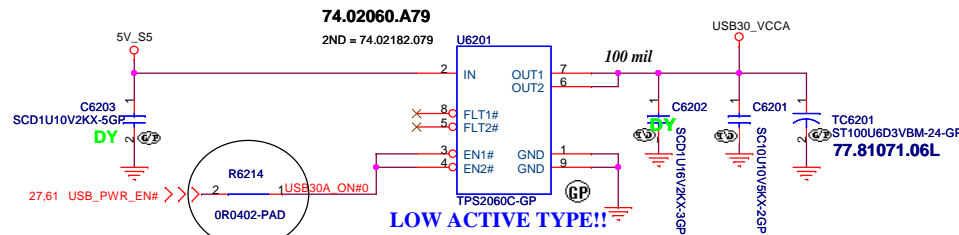
Colossus

Rev
1

Date: Wednesday, January 04, 2012

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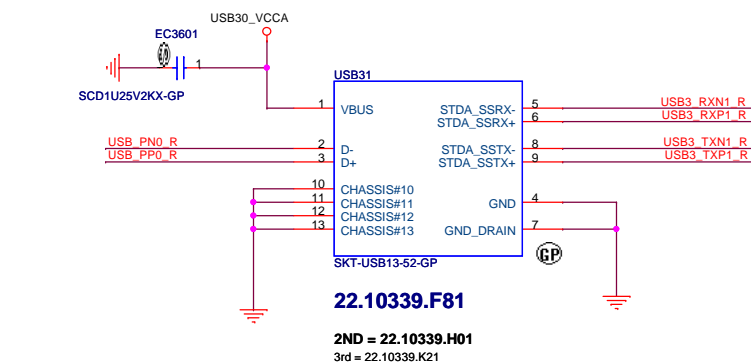
Power switcher Low active



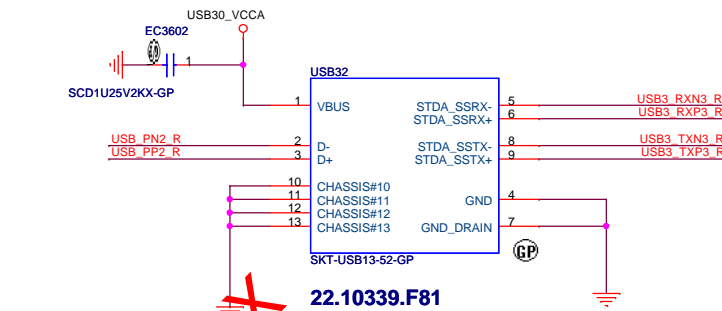
USB 3.0 Connector Pin definition

Pin	Signal
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+ SuperSpeed RX
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+ SuperSpeed TX

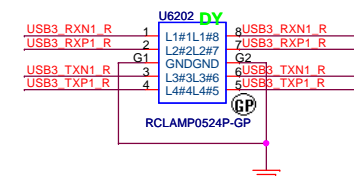
USB3_1



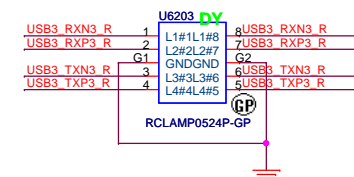
USB3_2



Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



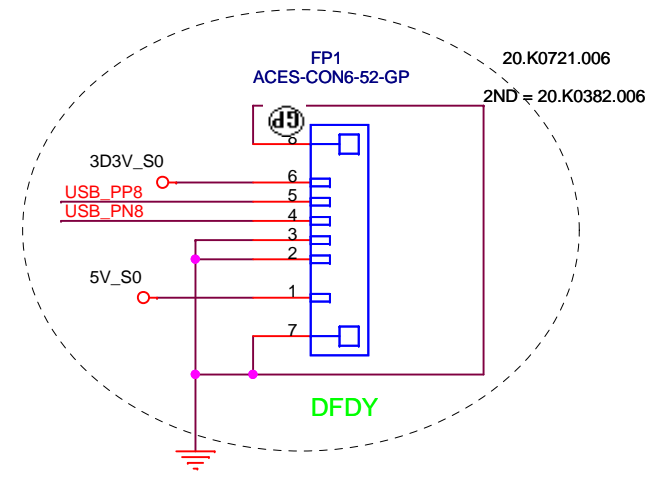
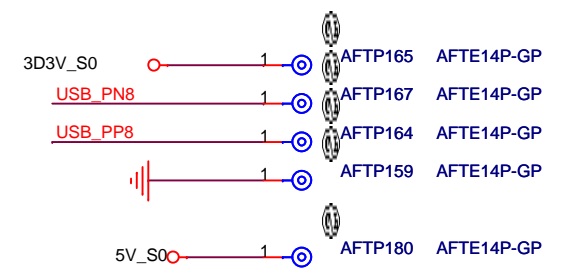
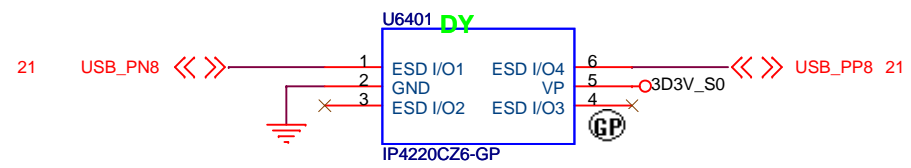
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
USB3.0		
Size	Document Number	Rev
A3	Colossus	1
Date:	Thursday, January 05, 2012	Sheet 62 of 103

Finger Printer

Eleto-X



-1 12/23 FP1 change source

<Core Design>

緯創資通			Wistron Corporation		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
Finger Print Conn					
Size A4	Document Number				Rev 1
Colossus					
Date: Wednesday, January 04, 2012					
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SSID = Wireless

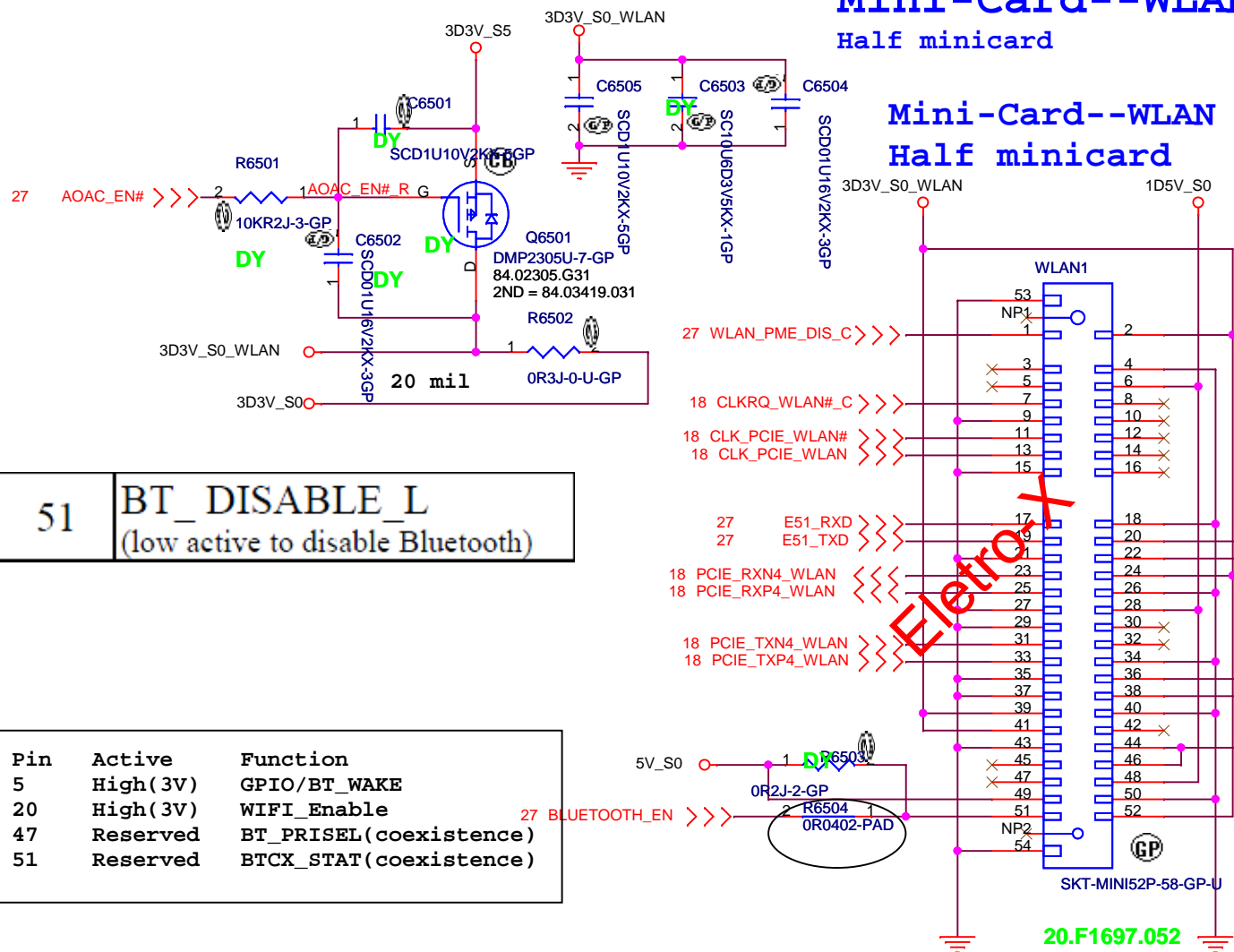
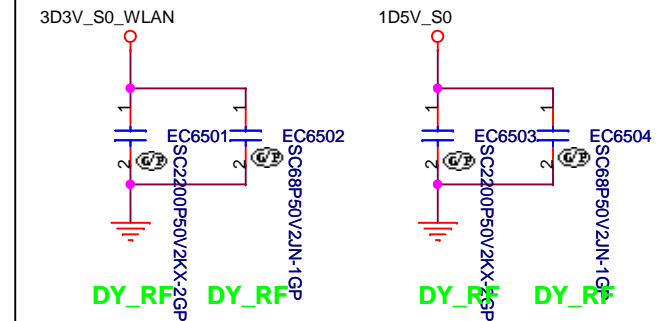
Mini-Card--WLAN

Half minicard

Mini-Card--WLAN

Half minicard

CLOSED IN WLAN1



51

BT_DISABLE_L

(low active to disable Bluetooth)

Pin	Active	Function
5	High(3V)	GPIO/BT_WAKE
20	High(3V)	WIFI_Enable
47	Reserved	BT_PRISEL(coexistence)
51	Reserved	BTCX_STAT(coexistence)

2ND = 20.F1697.052

3RD = Main:62.10043.F91

677869-FM8

1st	677869-FM8
2nd	677869-AM8
3rd	677869-BM8
4th	677869-LM8

<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

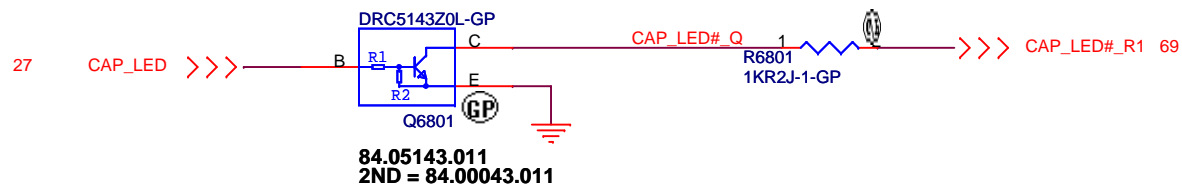
MINICARD(WLAN+Bluetooth)/CONN

Size	Document Number	Rev
A4	Colossus	1
Date:	Wednesday, January 04, 2012	Sheet 65 of 103

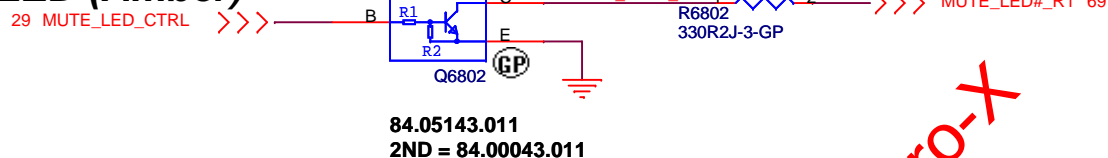
SSID = User.Interface

On Keyboard LEDs

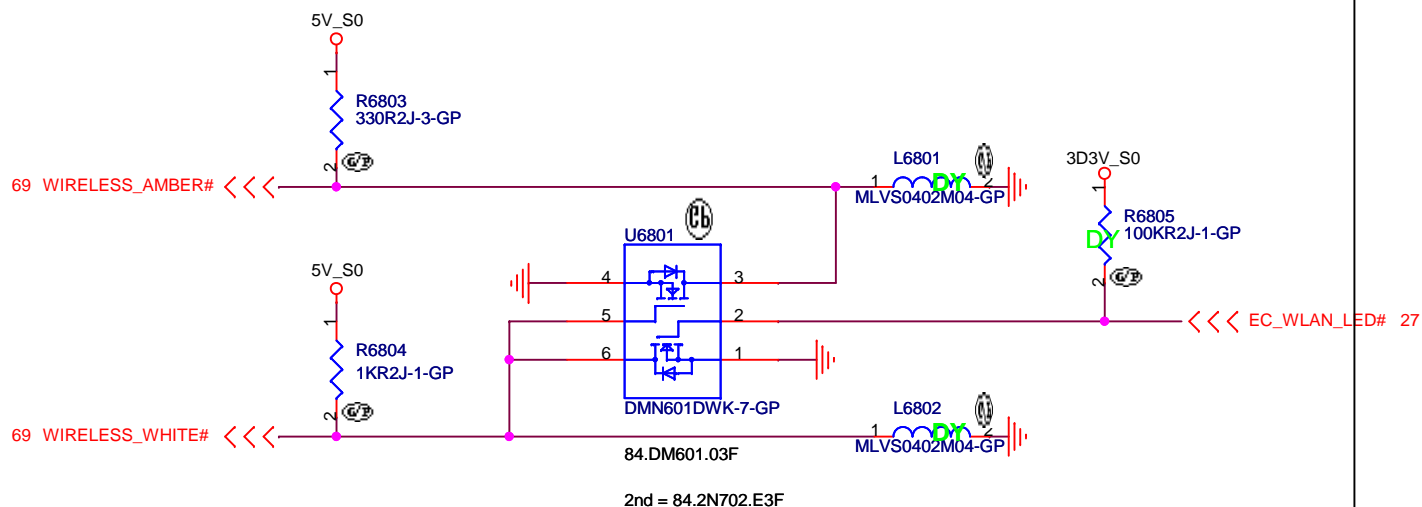
Cap locks LED (White)



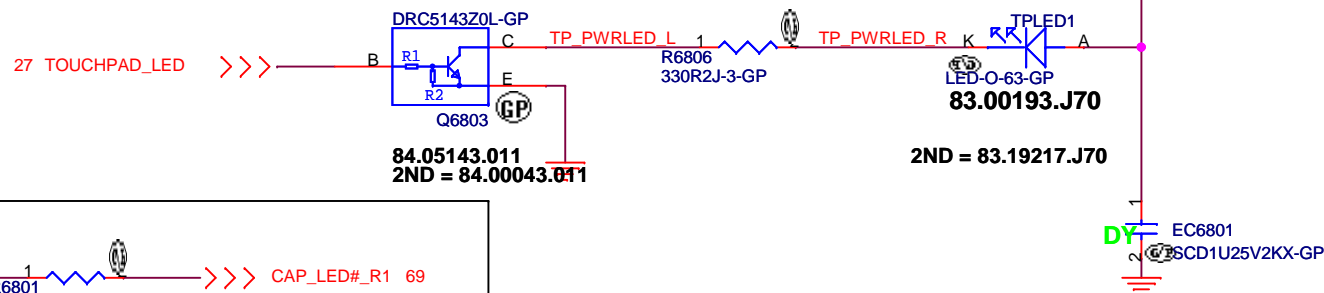
Mute LED (Amber)



Wireless LED (White-On, Amber-Off)



Touchpad LED (Amber)



Eleto-X

<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

LED Bard/Power Button

Size
A4

Document Number

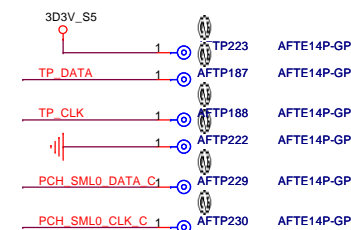
Colossus

Rev
1

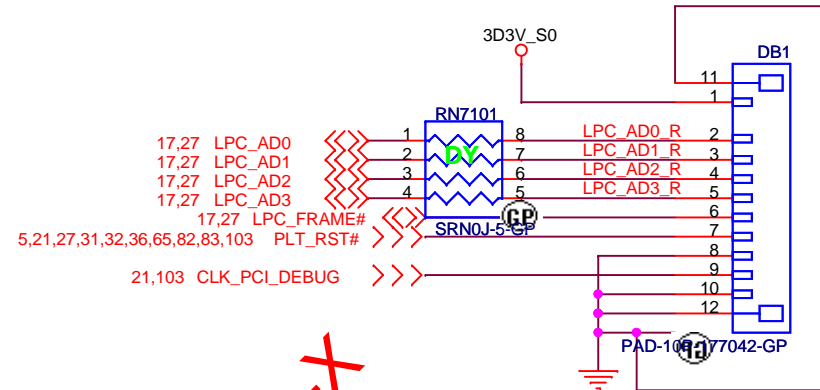
Date: Wednesday, January 04, 2012

Sheet 68 of 103

Internal KeyBoard Connector



DEBUG BD for Factory Test



ZZ.00PAD.Y41

-1 0102

<Core Design>

緯創資通

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Title

Dubug connector

Size
A4

Document Number

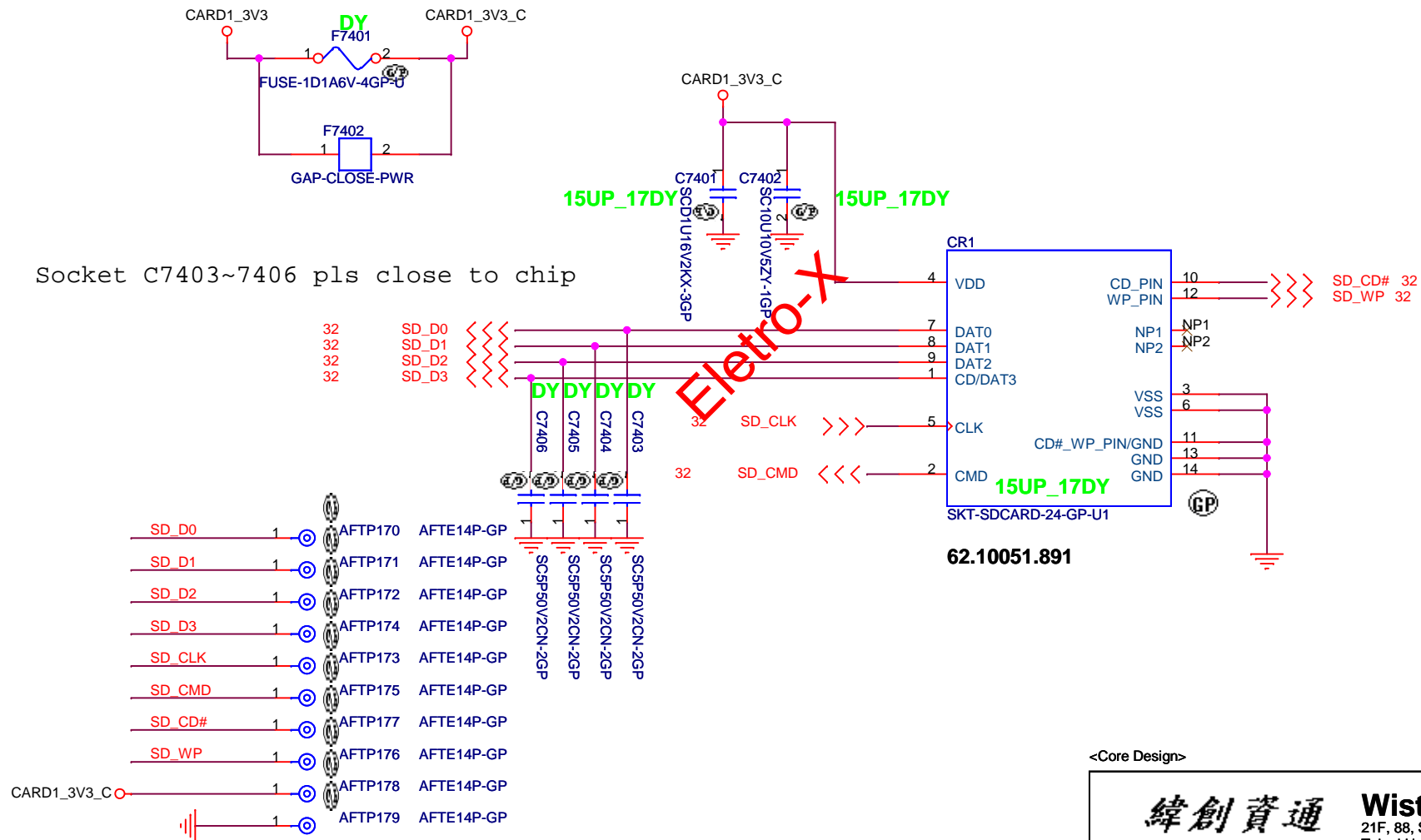
Colossus

Rev
1

Date: Wednesday, January 04, 2012

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2 IN1 CARD-READER (SD/MMC)



<Core Design>

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Title

CARD Reader CONN

Size
A4

Document Number

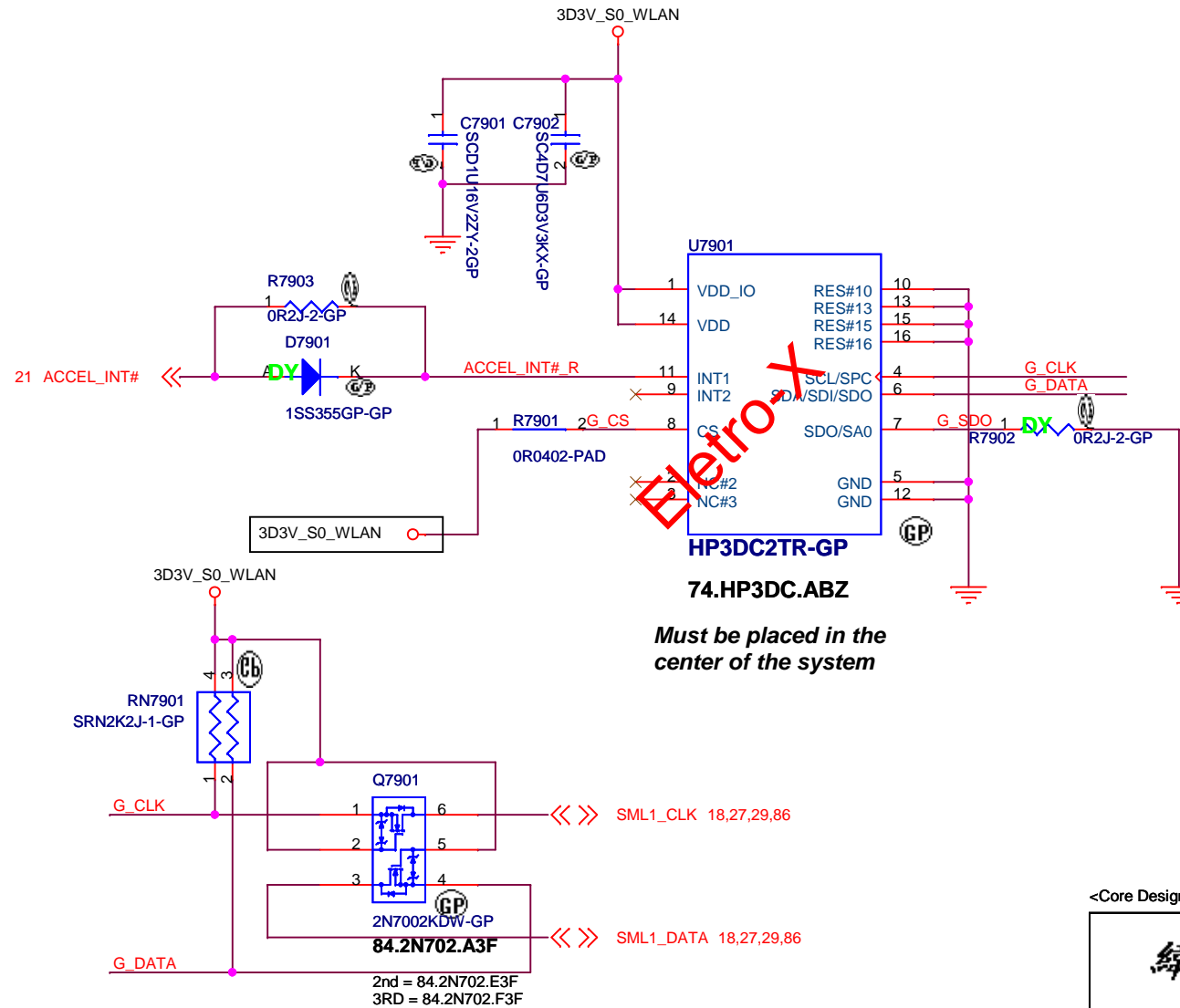
Colossus

Rev
1

Date: Wednesday, January 04, 2012

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ACCELEROMETER



Must be placed in the center of the system

<Core Design>

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Title

ACCELEROMETER

Size
A4

Document Number

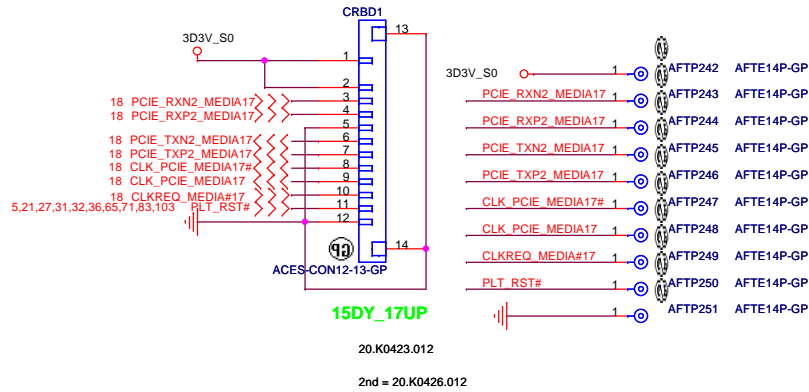
Colossus

Rev
1

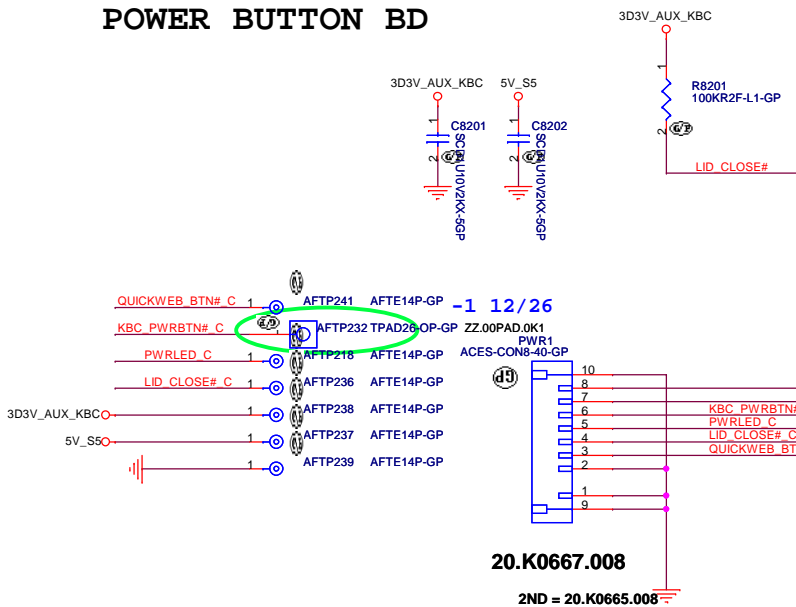
Date: Wednesday, January 04, 2012

Sheet	79	of	103
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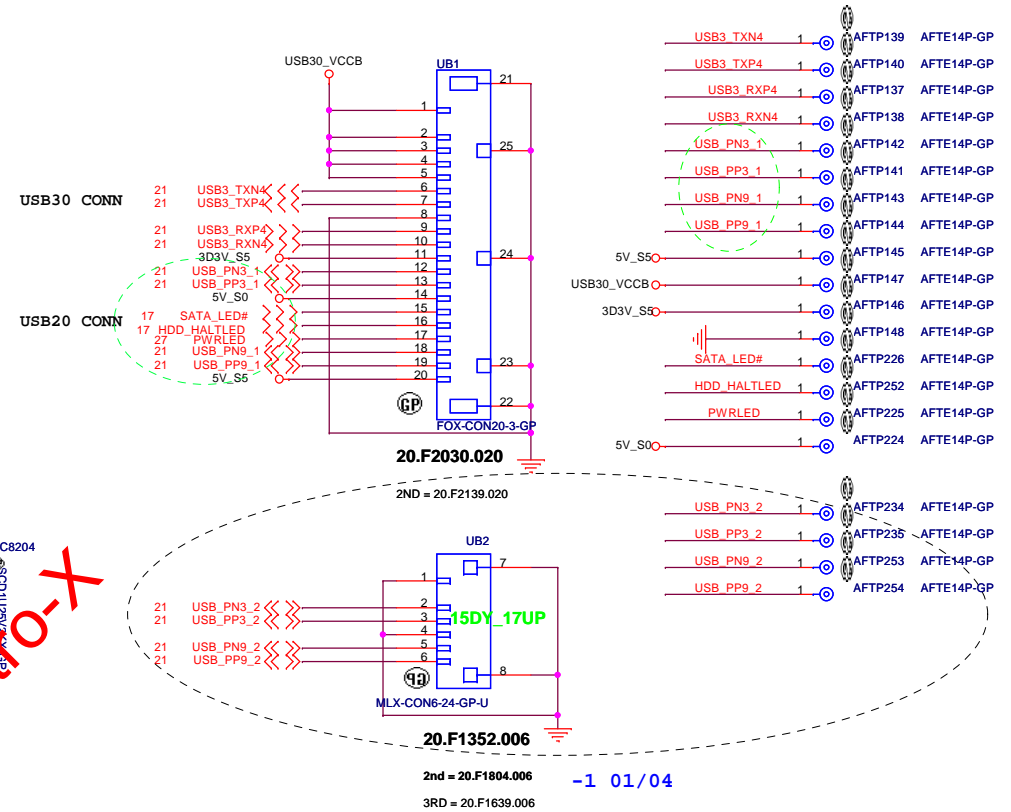
Card Reader BD 15"=DY 17"=PHASE IN



POWER BUTTON BD

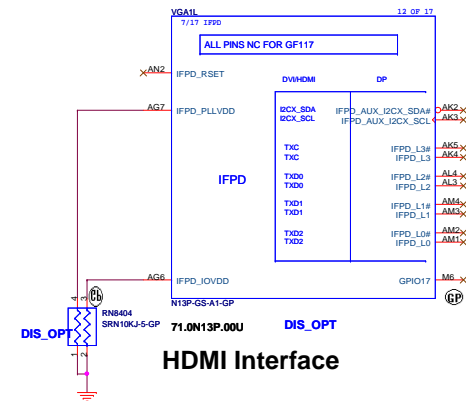
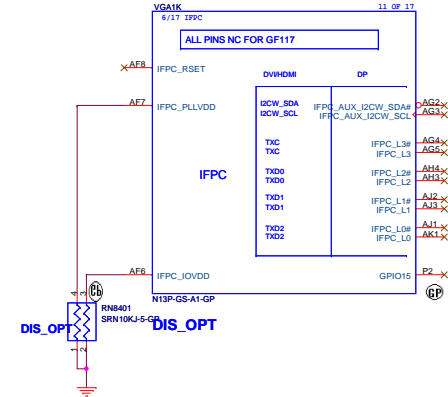
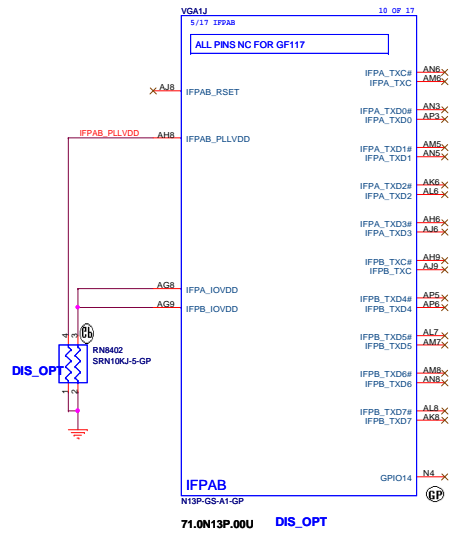


USB BD(USB3.0*1+USB2.0*1)

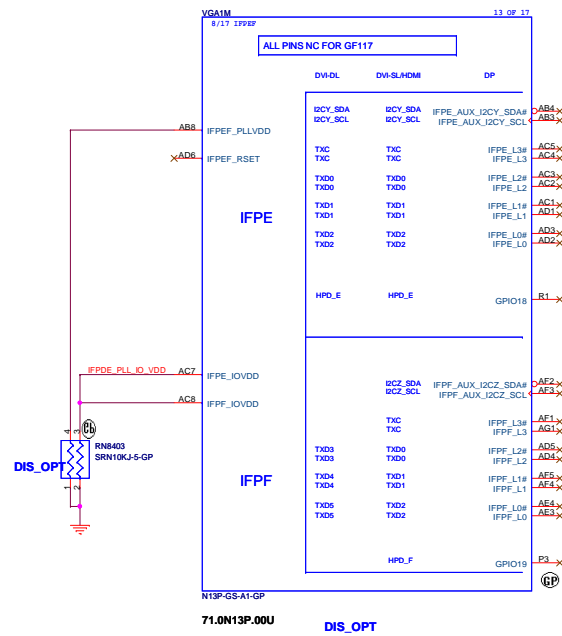


TOUCHPAD BD PAGE 69

LVDS Interface



HDMI Interface

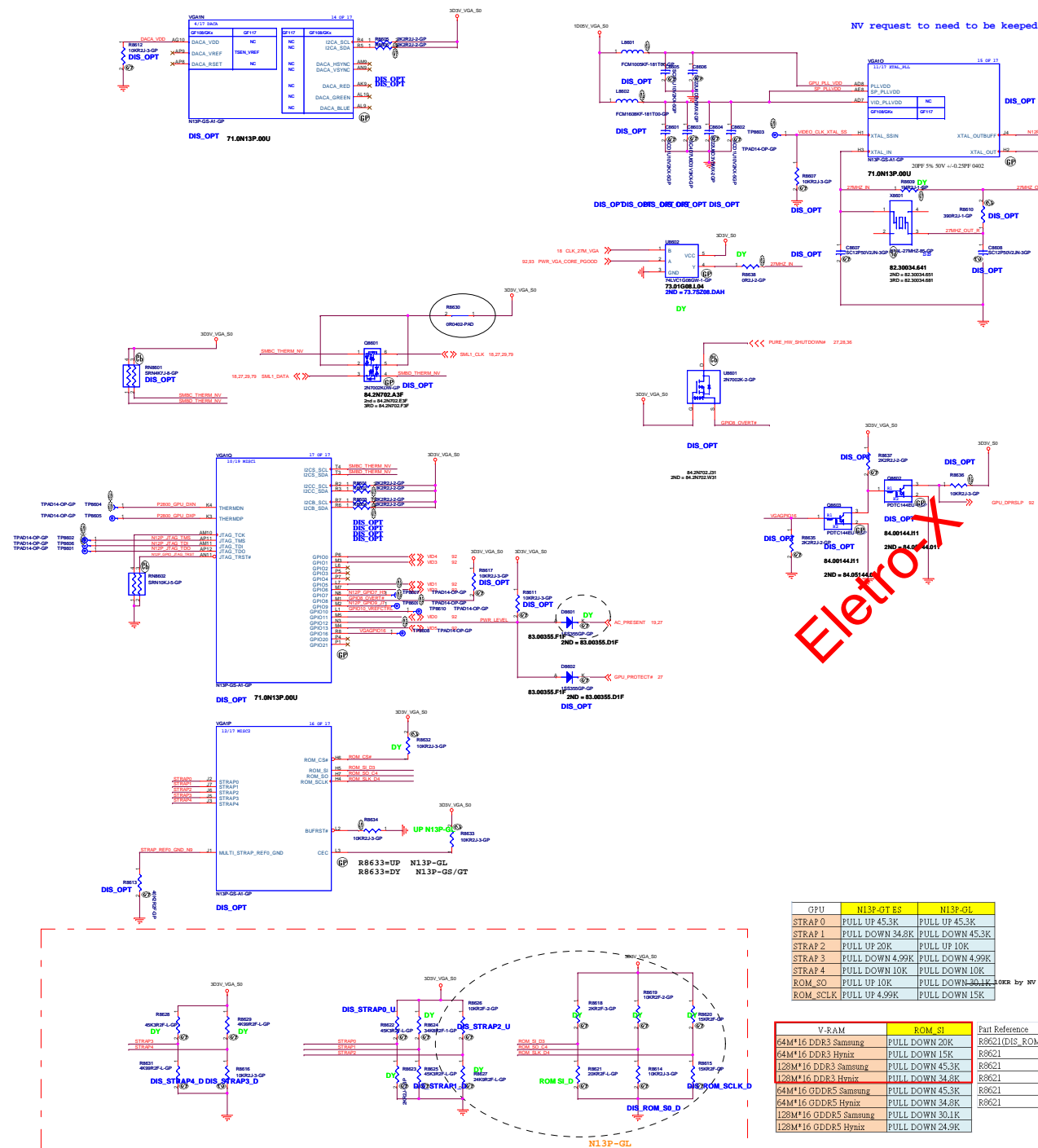


Eleto-X

<Variant Name>

緯創資通 Wistron Corporation
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Title			GPU Memory(2/5)
Size	Document Number	Rev	
A2	Colossus	1	
Date: Monday, December 26, 2011			Sheet 84 of 103



01/04/12 N13P-GL

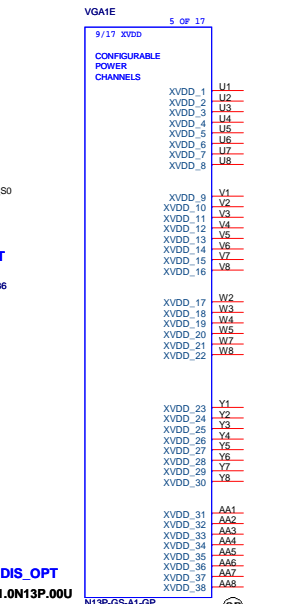
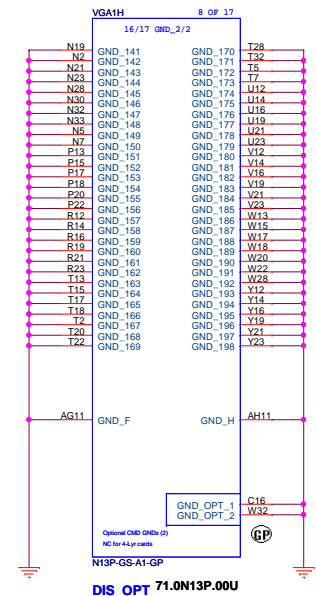
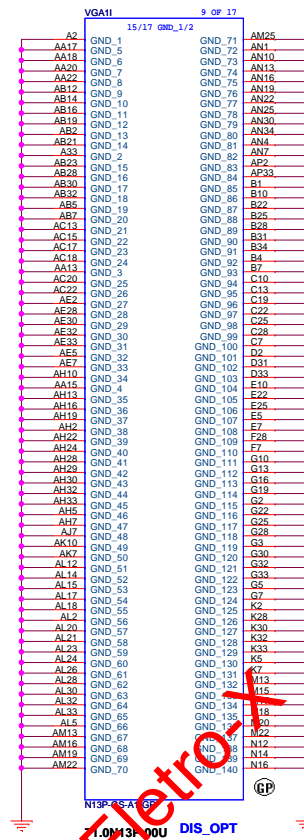
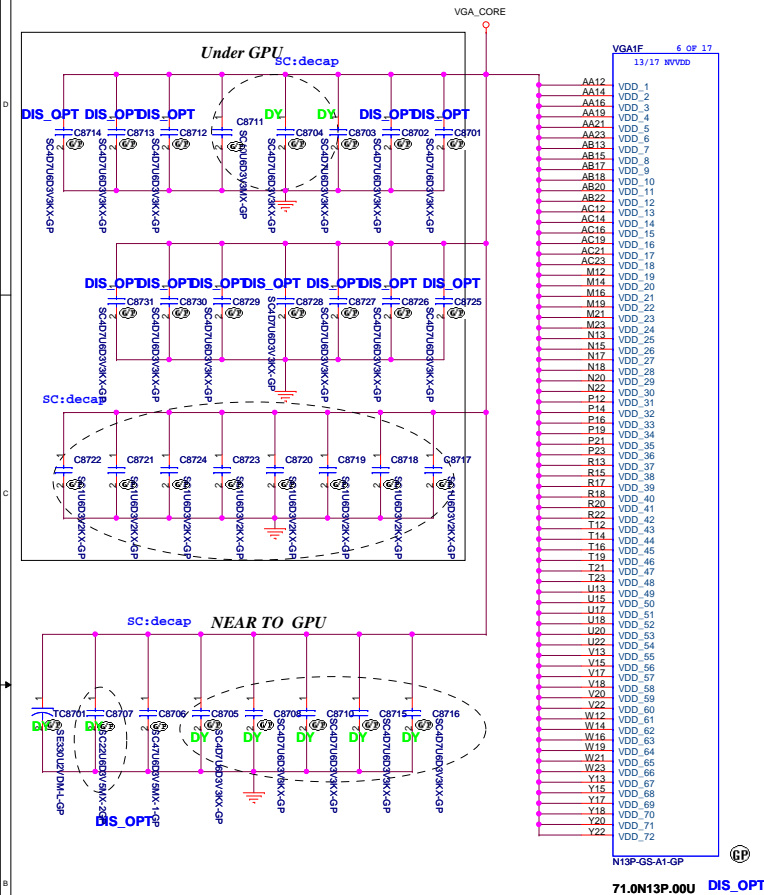
Strap Option for N13P-GL/LP/GS/GT

Strap Name	GPU SKU	Logical strapping name bit#3	Logical strapping name bit#2	Logical strapping name bit#1	Logical strapping name bit#0	Set your BOM according to this column	Comment from NVIDIA
ROM_S0	N13P-GL	0	0	0	0	PULL DOWN 10K	
	N13P-LP	0	0	0	1	PULL DOWN 10K	
	N13P-LP	1	0	0	1	PULL UP 10K	
	N13P-GS	1	0	0	1	PULL UP 10K	
	N13P-GT	1	0	0	1	PULL UP 10K	
	N13M-GE1	0	1	0	1	PULL DOWN 30.1K	
ROM_SCLK	N13P-GL	0	0	1	0	PULL DOWN 15K	
	N13P-LP	0	0	1	0	PULL DOWN 15K	
	N13P-LP	1	0	0	0	PULL UP 4.99K	
	N13P-GS	1	0	0	0	PULL UP 4.99K	
	N13P-GT	1	0	0	0	PULL UP 4.99K	
	N13M-GE1	0	1	0	0	PULL UP 4.99K	
ROM_SI	N13P-GL	0	0	0	0	PULL DOWN 10K	
	N13P-LP	0	0	0	0	PULL DOWN 10K	
STRAP2	N13P-GL	1	0	0	1	PULL UP 10K	N13P-GL DID => 0x0DE9
	N13P-LP	0	0	1	1	PULL UP 4.99K	N13P-LP DID => 0x0DE9
	N13P-LP	0	0	1	1	PULL DOWN 20K	N13P-GS DID => 0x0F03
	N13P-GS	0	1	0	0	PULL DOWN 15K	N13P-GS DID => 0x0F03
	N13P-GT	0	1	0	0	PULL DOWN 10K	N13P-GT DID => 0x0F03
	N13M-GE1	1	0	0	0	PULL UP 4.99K	N13M-GE1 DID => 0x0F03
STRAP1	N13P-GL	0	1	1	1	PULL DOWN 45.3K	
	N13P-LP	0	1	1	1	PULL DOWN 45.3K	
	N13P-LP	0	1	1	0	PULL DOWN 34.8K	
	N13P-GS	0	1	1	0	PULL DOWN 34.8K	
	N13P-GT	0	1	1	0	PULL DOWN 34.8K	
	N13M-GE1	0	1	1	0	PULL DOWN 45.3K	
STRAP0	N13P-GL	1	1	1	1	PULL UP 45.3K	
	N13P-LP	1	1	1	1	PULL UP 45.3K	
	N13P-LP	1	1	1	1	PULL UP 45.3K	
	N13P-GS	1	1	1	1	PULL UP 45.3K	
	N13P-GT	1	1	1	1	PULL UP 45.3K	
	N13M-GE1	1	1	1	1	PULL UP 45.3K	
STRAP3	N13P-GL	0	0	0	0	PULL DOWN 4.99K	
	N13P-LP	0	0	0	0	PULL DOWN 4.99K	
	N13P-LP	0	0	0	0	PULL DOWN 4.99K	
	N13P-GS	0	0	0	0	PULL DOWN 4.99K	
	N13P-GT	0	0	0	0	PULL DOWN 4.99K	
	N13M-GE1	0	0	0	0	PULL DOWN 4.99K	
STRAP4	N13P-GL	0	0	0	0	PULL DOWN 10K	
	N13P-LP	0	0	0	0	PULL DOWN 10K	
	N13P-LP	0	1	1	1	PULL DOWN 45.3K	
	N13P-GS	0	1	1	1	PULL DOWN 45.3K	
	N13P-GT	0	1	1	1	PULL DOWN 45.3K	
	N13M-GE1	0	0	0	0	PULL DOWN 10K	

GPU	N13P-GT ES	N13P-GL
STRAP 0	PULL UP 45.3K	PULL UP 45.3K
STRAP 1	PULL DOWN 34.8K	PULL DOWN 45.3K
STRAP 2	PULL UP 20K	PULL UP 10K
STRAP 3	PULL DOWN 4.99K	PULL DOWN 4.99K
STRAP 4	PULL DOWN 10K	PULL DOWN 10K
ROM_S0	PULL UP 10K	PULL DOWN 30.1K
ROM_SCLK	PULL UP 4.99K	PULL DOWN 15K

V-RAM	ROM_SI
64M*16 DDR3 Samsung	PULL DOWN 20K
64M*16 DDR3 Hynix	PULL DOWN 15K
128M*16 DDR3 Samsung	PULL DOWN 45.3K
128M*16 DDR3 Hynix	PULL DOWN 34.8K
64M*16 GDDR5 Samsung	PULL DOWN 45.3K
64M*16 GDDR5 Hynix	PULL DOWN 34.8K
128M*16 GDDR5 Samsung	PULL DOWN 30.1K
128M*16 GDDR5 Hynix	PULL DOWN 24.9K

EDP 60A (TDP 55W)

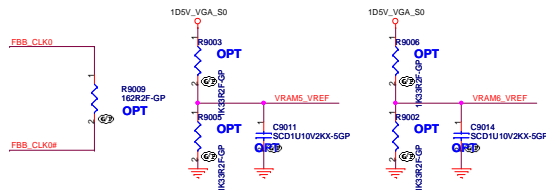
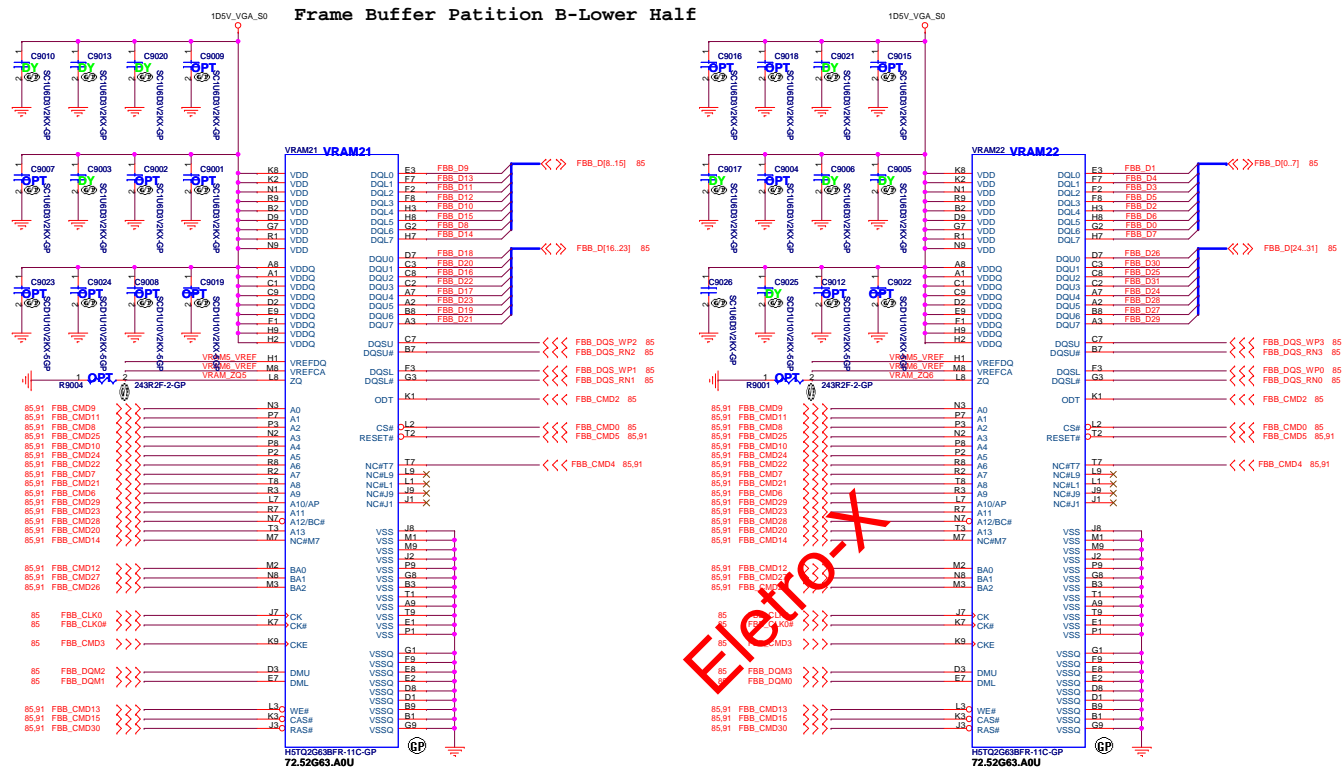


XVDD_1~38=No Connect

<Variant Name>

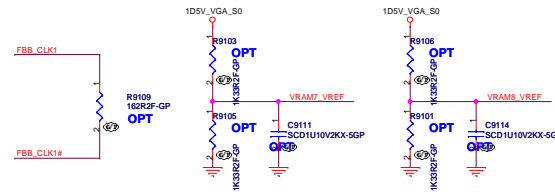
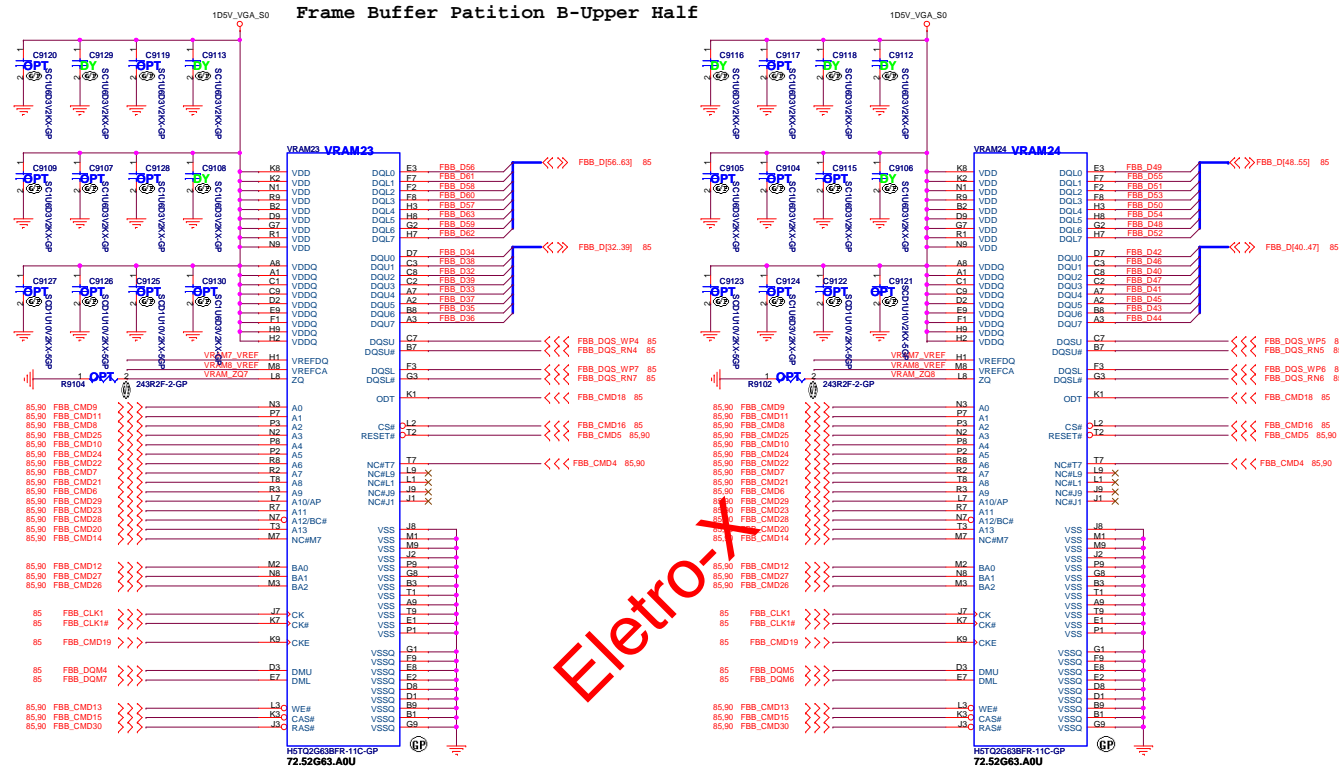
緯創資通 Wistron Corporation 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
GPU_DPPWR/GND(5/5)	
Title Size Customer Date:	Document Number Colossus Wednesday, January 04, 2012
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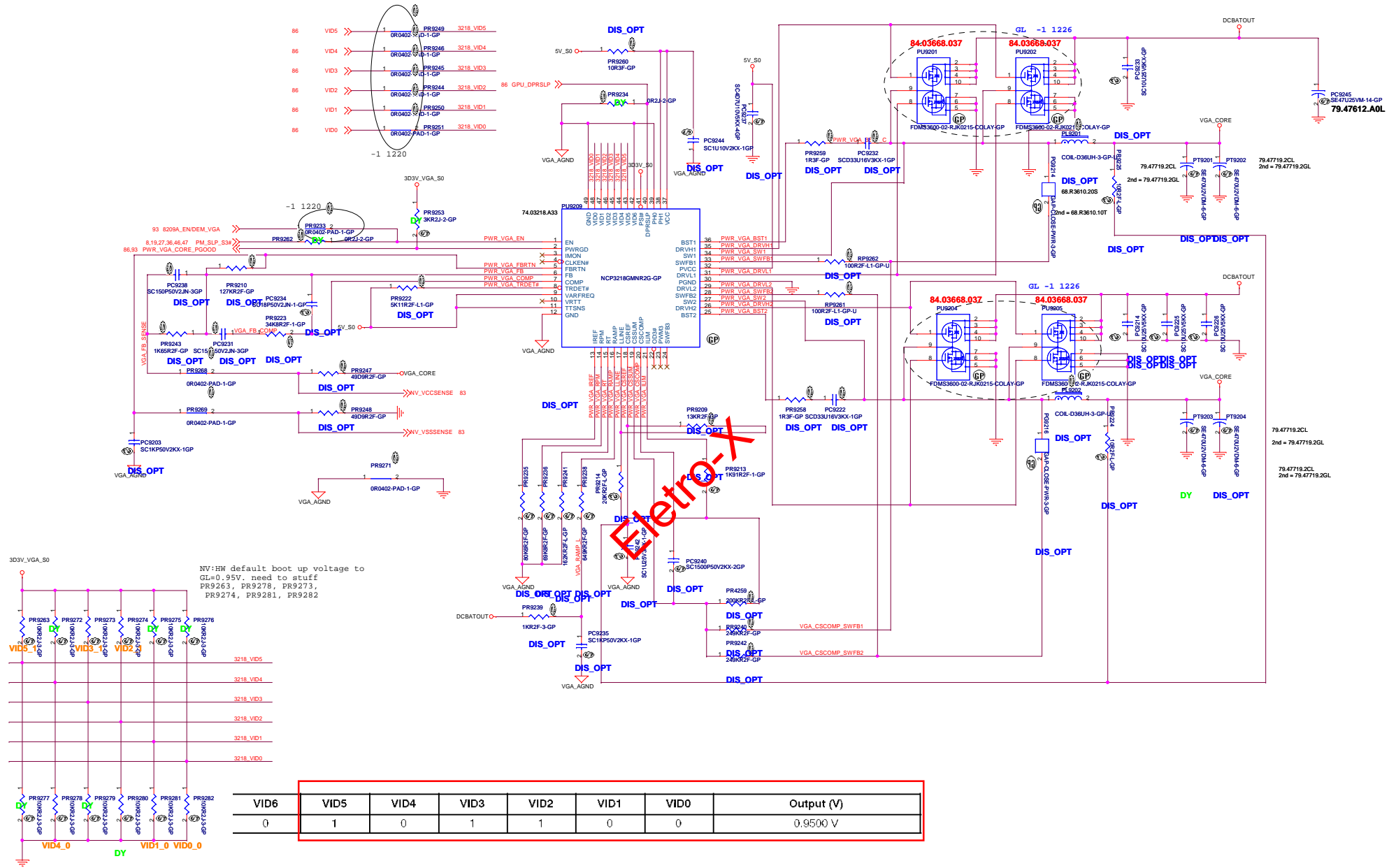




<Variant Name>

Frame Buffer Patition B-Upper Half



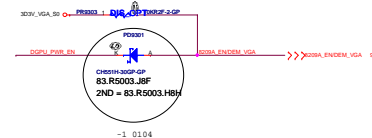
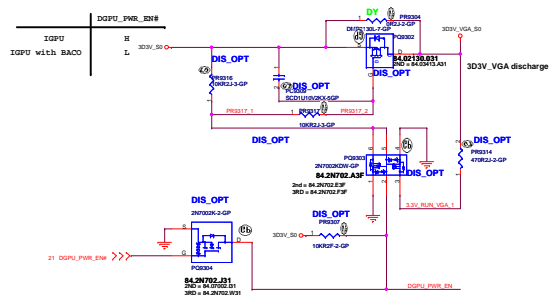


VGA chip sequence: 3V_VGA_S0>VGA_CORE>1D5V_VGA>1D05V_VGA

3V_VGA_S0

VGA_CORE

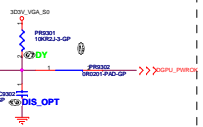
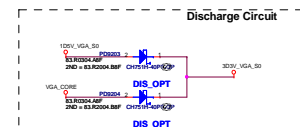
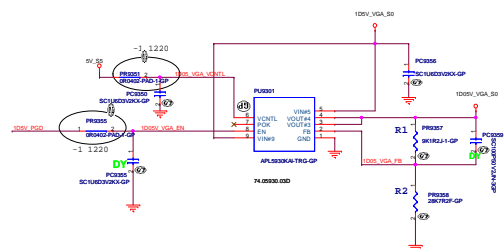
1.5V_VGA_S0



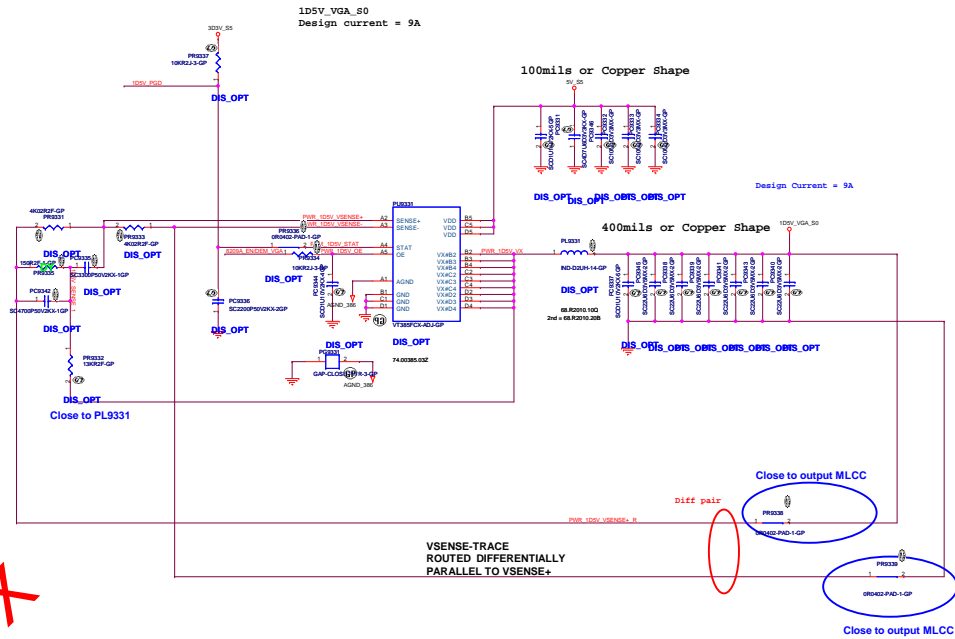
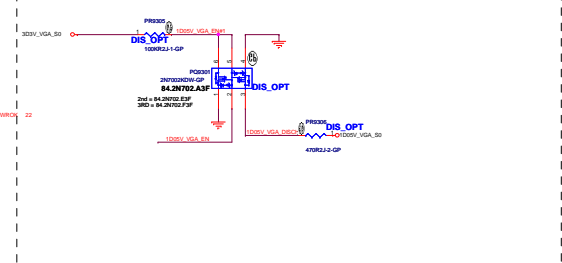
1D05V_VGA

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D5V_VGA_S0 should ramp up
so 1D05V_VGA_S0 EN have to fine tune RC delay
after VGA_Core

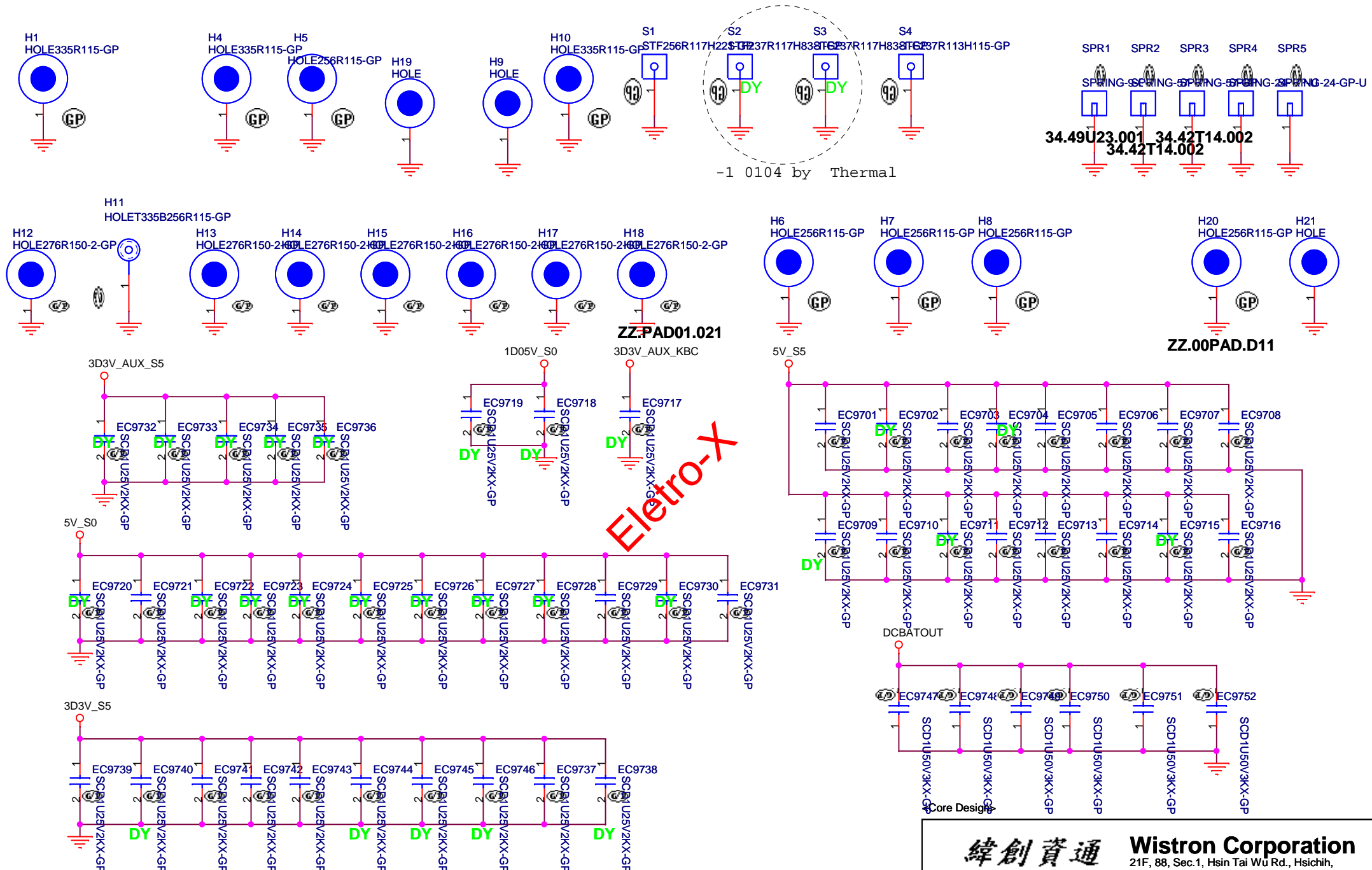
1D05V_VGA_S0
Design current = 3.8A



Discharge Circuit



Eleto-X



34.49U23.001 34.42T14.002
34.42T14.002

Electro-X

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

UNUSED PARTS/EMI Capacitors

Size A4

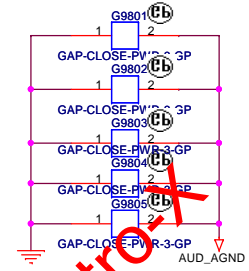
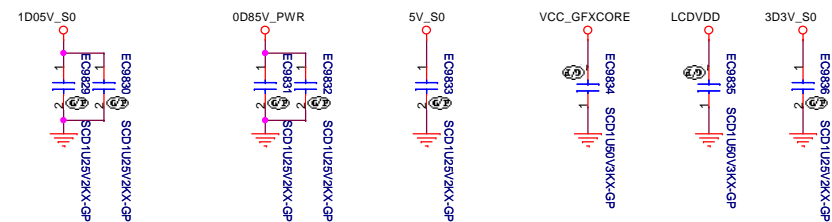
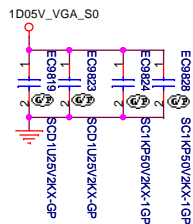
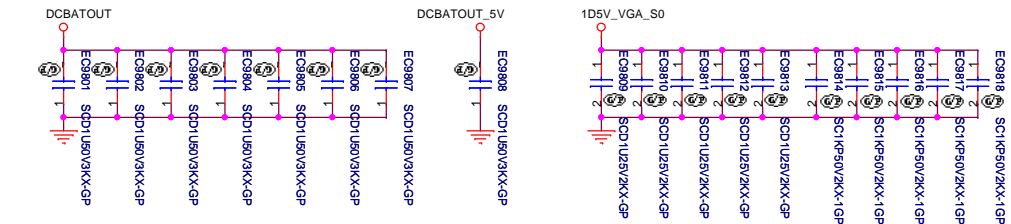
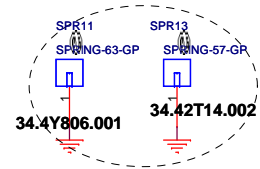
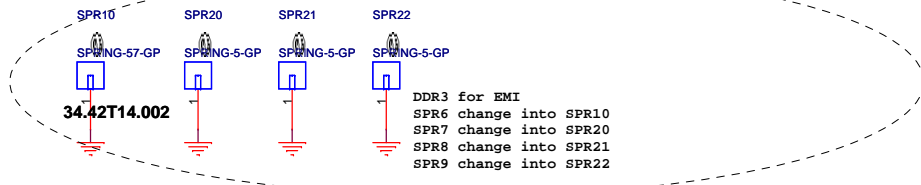
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Rev 1

Date: Wednesday, January 04, 2012

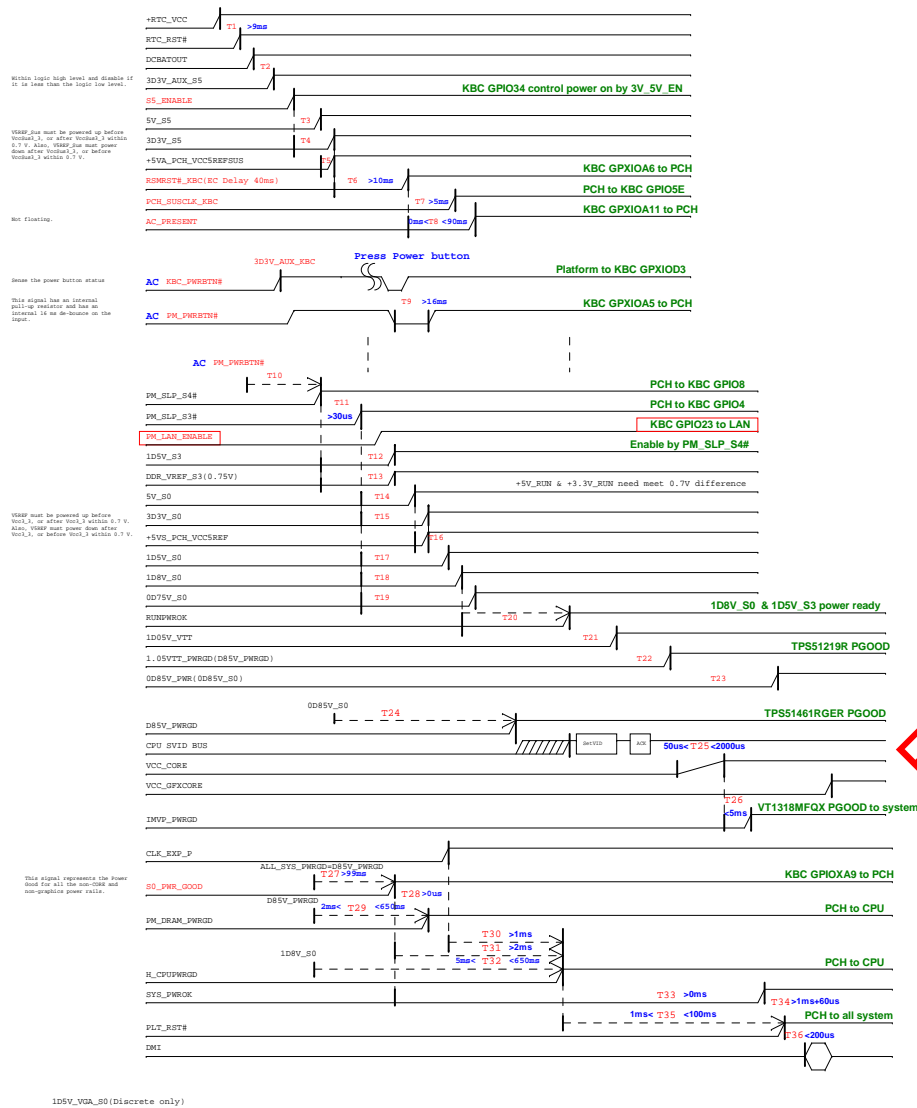
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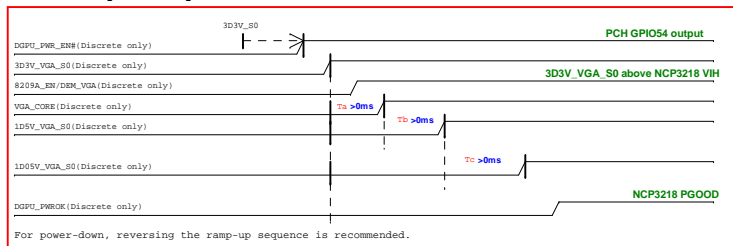
Chief River Platform Power Sequence

(AC mode)

red word: KBC GPIO



N13P Power-Up/Down Sequence



(DC mode)

red word: KBC GPIO

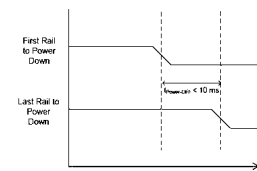
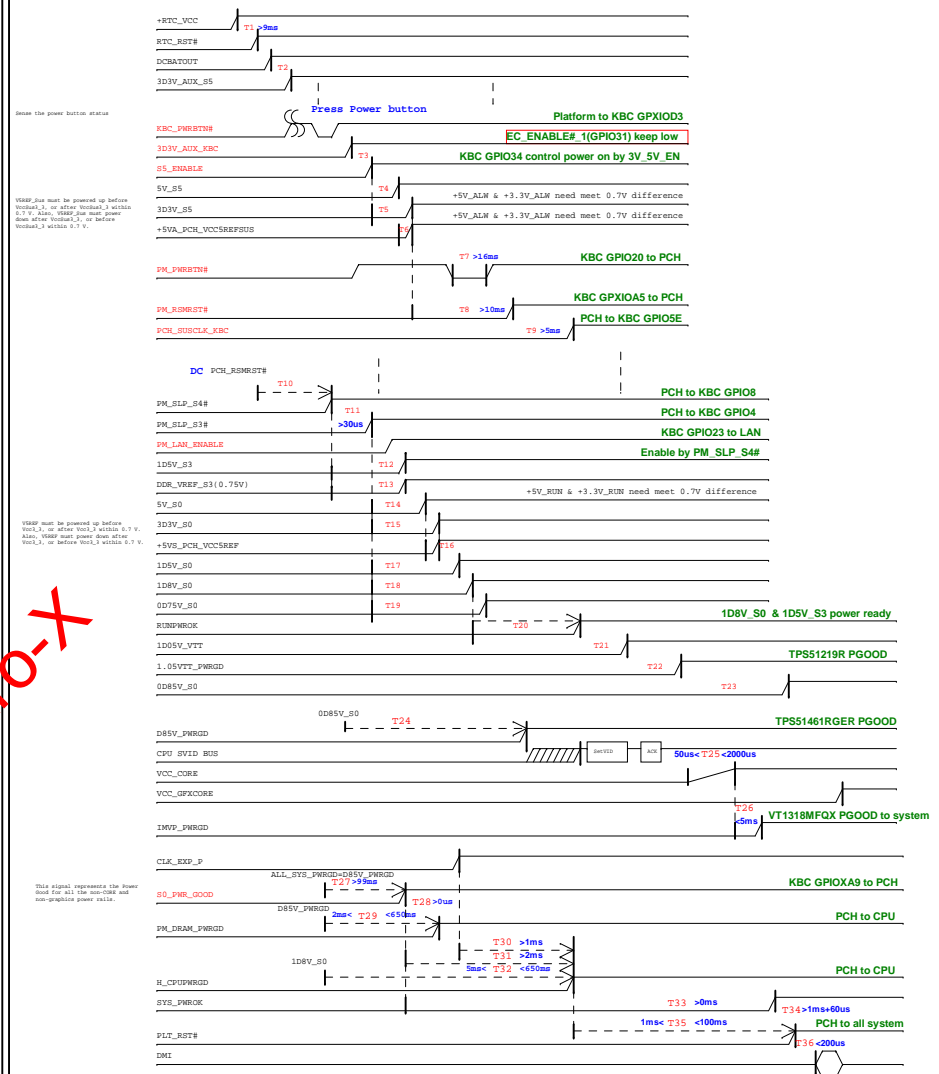
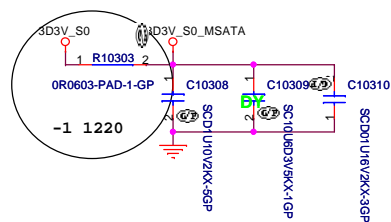
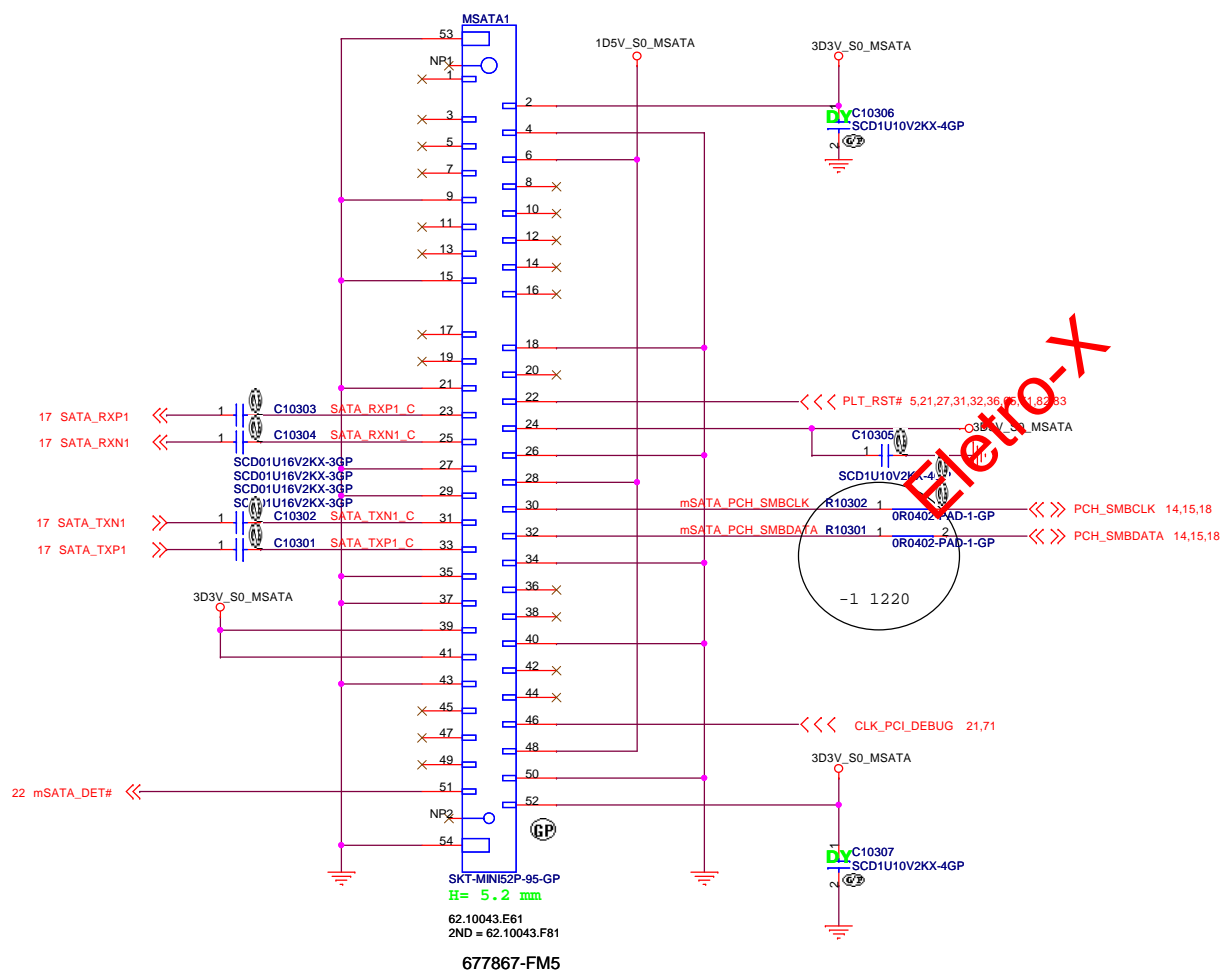
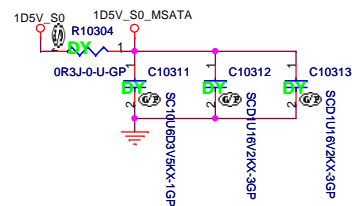


Figure 18. Recommended Power Off Sequencing Order



mSATA



1st 677867-FM5
2nd 677867-AM5
3rd 677867-BM5
4th 677867-LM5

Pin #	Name	Description	Pin #	Name	Description
1	Reserved	NC	2	V33	3.3V power
3	Reserved	NC	4	GND	Return Current Path
5	Reserved	NC	6	V15	1.5V power (Unused)
7	Reserved	NC	8	Reserved	NC
9	GND	Return Current Path	10	Reserved	NC
11	Reserved	NC	12	Reserved	NC
13	Reserved	NC	14	Reserved	NC
15	GND	Return Current Path	16	Reserved	NC
Key					
17	Reserved	NC	18	GND	Return Current Path
19	Reserved	NC	20	Reserved	NC
21	GND	Return Current Path	22	Reserved	NC
23	B+	Differential Signal Pair B (Device Tx)	24	V33	3.3V power
25	B-		26	GND	Return Current Path
27	GND	Return Current Path	28	V15	1.5V power (Unused)
29	GND	Return Current Path	30	Reserved	NC
31	A-	Differential Signal Pair A (Device Rx)	32	Reserved	NC
33	A+		34	GND	Return Current Path
35	GND	Return Current Path	36	Reserved	NC
37	GND	Return Current Path	38	Reserved	NC
39	V33	3.3V power	40	GND	Return Current Path
41	V33	3.3V power	42	Reserved	NC
43	GND	Return Current Path	44	Reserved	NC
45	Vendor	No connect at Host side	46	Reserved	NC
47	Vendor	No connect at Host side	48	V15	1.5V power (Unused)
49	DAS/DSS	Drive Activity Signal	50	GND	Return Current Path
51	Presense	Device Presense	52	V33	3.3V power

Note: 1: DAS/DSS signal is not use for this drive. (DAS Signal output is optional)

*2: Presense pin is Connected to GND by device side. (220 Ω Pull Down)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

mSATA

Size
A3

Document Number

Colossus

Rev
1

Date: Wednesday, January 04, 2012

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